Parametric simulation of SiC Schottky JBS structures

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Abstract

The parametric simulation has been carried out for optimizing the influence of the Schottky contact metal work function (contact surface interface) influence on the distribution of the built-in electrical field and consequently on static and dynamic characteristics of the JBS device. On the basis of simulations and discussions the low-power losses solution for the JBS device has been developed. The results suggest keeping the electric field strength under contact surface as low as possible in order to reduce or even avoid the relatively expensive and complex passivation solutions by the manufacturing of the JBS devices.

The numerical simulator DYNAMIT 2DT-SCHOTTKY developed at the Department of Electronics TUT was used in our research.
Keywords: SiC, JBS structures, contact metal work function, numerical modelling.

1 Introduction

Silicon carbide (SiC) is an outstanding compound semiconductor material with extremely promising physical properties that make it an excellent candidate in high-speed and high-temperature power electronic applications. Metal semiconductor interface is a fundamental aspect in any semiconductor device technology. The research of different characteristics of Schottky contact involved semiconductor structures is important. Furthermore, the 4H- and 6H- polytypes of SiC have some remarkably different parameters, which have direct influence on device characteristics.

The authors of this paper have studied devices with different Schottky barriers for a long time. The changes in barrier heights strongly influence the

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current transport in Schottky interfaces and the investigation results are shown for example in [1, 2]. There are many aspects in simple Schottky devices, which are similar to ones in JBS (e.g. current crowding phenomenon). From another point of view the JBS devices have specific advantages compared to traditional simple *pn-* or Schottky devices. Many experimental results dealing with simulation of JBS devices have been published (e.g. [3-8]). Almost all simulation reports discuss only about the best relation of *pn-* and Schottky areas, and only some of the reports deal with the different Schottky contact properties (barrier height, size), placing of implanted regions, geometrical dimensions and doping concentration of drift region. There have been no papers about JBS devices based on *p*-type SiC. The processes inside of JBS devices have been poorly investigated. The electric field strength distribution and minority carrier distribution in the devices have been studied. Those studies have been done only for certain parts inside the device and in one dimension. In this paper we make an attempt to bridge this gap in some specific aspects.

The simulations have been done with simulation software SIC-DYNAMIT-2DT SCHOTTKY, developed at TUT Department of Electronics [9, 10], aided by bash shell scripts for automation of simulations and gnu-plot for presenting the results.

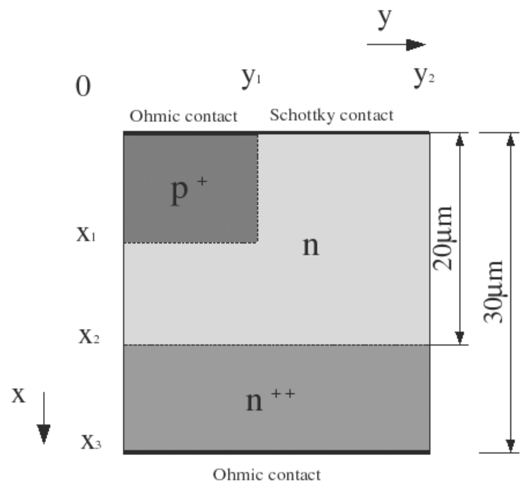

Figure 1: The device under study.

2 Description of the model

The simulations were performed on 6H-SiC and 4H-SiC Junction Barrier Schottky (JBS) structures (Fig. 1). Its dimensions and parameters were changed repeatedly to study the influence of those changes to electrical parameters and characteristics of the device.

The parameters of device are: width of the device (y_2) varies between 1 and 15 μm, width of p^+ area (y_1) between 0.25 and 5 μm, depth (x_1) is chosen to be between 1 and 20 μm and acceptor doping concentration 5×10^{16} cm^{-3}, epitaxial layer (n area) depth (x_2) 20 μm with donor doping concentration between 1×10^{15} and 4×10^{15} cm^{-3}, part of the substrate (n^{++} area) depth (x_3–x_2) 10 μm with donor doping concentration 1×10^{19} cm^{-3}, Schottky contact metal work function varies between 5.1 and 5.7 V, and ambient temperature gap lies between 300 and 900 K. The area of the device was chosen to be always 1 cm^2, to equal current and current density. Complementary p semiconductor based device data correspond to previously described ones.

Avalanche ionization coefficients of SiC semiconductor were taken from [11].

The Shockley–Roosbroeck system containing Poisson's equation, charge carriers continuity and transport equations with additional Maxwell's total current equation is used. The Electron Hole Scattering (EHS) effect is introduced in *SIC-DYNAMIT-2DT* simulation package. Additional coefficients are used for high electron and hole concentrations. Mobility dependence on doping concentration, temperature, electrical field, and on the concentration of charge carriers is used. Boundary conditions for Ohmic and Schottky interfaces are described as it is shown for example in reference [10].

The detailed description of the model used here is presented in [12], the appropriate model parameters are presented in our latest paper on this topic [13], and therefore these questions will be not discussed here in more detail.

3 Results and discussion

Many practical examples of SiC JBS devices have been introduced. Still it is difficult to find the comparable examples, where the experimental results of manufactured devices match well with the simulation results, particularly with the results of our simulations. The reason for that is rather simple. The so called best device defined on base of our investigations should have very deep emitter area, which is unfortunately very difficult to realize with today's SiC device manufacturing technologies. So, our results presented here have therefore the meaning of the so called best theoretical device. Of the physically manufactured devices, the closest to our results is the one proposed by Rutgers University, USA. The experimental results are presented in the paper [14]. This device is to the best of our knowledge the demonstrator with the best electrical properties presented till today. The geometrical and electrical parameters of this device are presented in [14] as well. To validate our model with best experimental data some critical results from the point of view of device behavior were investigated earlier and the part of comparable results are presented in our earlier work [12]. Here we continue to report our latest simulation results.

Firstly, we comment the full dimensions of the JBS device. The forward characteristics depend not only on relative dimensions (ratio of *pn*-junction area to the Schottky junction area) of the device, but also on the absolute dimensions of the device parts as well. The device with the smallest dimensions can conduct much lower forward current compared with other examined devices. The reason stems directly from the screening behavior of Schottky part (about 0.66 µm) of the device by the *pn*-part. The similar situation is followed with applied reverse voltage too, which means that the *pn* part of the device defines the current at low voltages (Fig. 2). It is important to state that at the smallest ratio of the Schottky and *pn*–junction the Schottky area leakage current is almost completely blocked under 1000 V and JBS device conducts the leakage current of *pn*-junction. The lower breakdown voltage in case of the smallest device (about 15 µm) is caused by higher electric field strength in semiconductor volume near the emitter bottom region (Fig. 3). This is clearly seen on Fig. 4, where the electric field strength dependence on device dimensions is presented. It is seen that in case of the highest simulated dimensions the effect of the lowering electric field strength under Schottky contact is very weak. Similar behavior has been seen also in the case of the smallest devices (about 3 µm). The latter situation concludes from the limited propagation of depletion region of *pn*-junction.

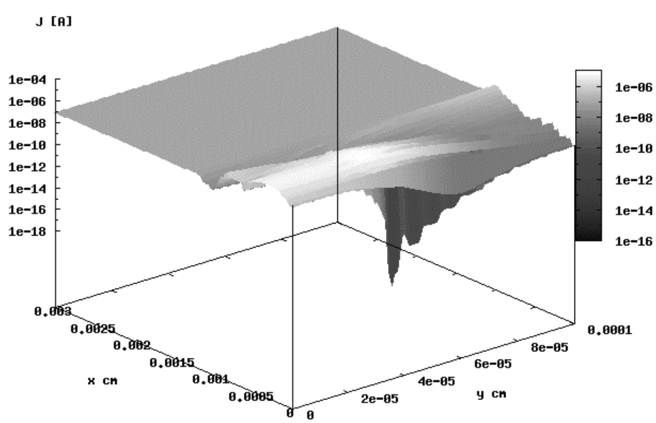

Figure 2: Current crowding to *p* area at U_F=0.2V, device size 1 µm.

Our simulations show clearly that the turn-off time depends weakly on device final dimensions. The small difference in turn-off time values seems to be caused by the ratio of the depleted region to conducting area of Schottky part. Depleted region edge around the emitter area is the same for all dimensions, but the Schottky area dimensions are changing. From this situation we conclude that although the Schottky area ratio for the whole device area is not changing, the conducting Schottky area ratio to the whole device area is higher at larger device dimensions and the turn-off time increases minimally (less than 3% compared to shortest turn-off times of the device).

The next important topic is the variation of the Schottky contact metal work function and its influence on forward and reverse characteristics, and on the distribution of the electrical field strength and the turn off time. The unique *p*-substrate structure is under the investigations. The behaviour of the forward and reverse characteristics is shown in Fig. 5. The work function has remarkable influence on forward characteristics (Fig. 5) through influence on the height of Schottky barrier. The influence is clearly seen at low voltage values as then the majority of the total current is conducted by the Schottky part of the device. On higher voltages most of the current flows through the *pn*-part of the device and the influence of the Schottky barrier loses its importance. Also the influence of the work function on reverse characteristics (Fig. 6) is remarkable. Namely, the lower Schottky contact metal work function causes higher leakage current values in the Schottky part of the device and therefore in the whole device as well.

On the base of the results of the simulations we state that the electric field strength distribution and the turn-off time of the device are almost not influenced by the contact metal work function.

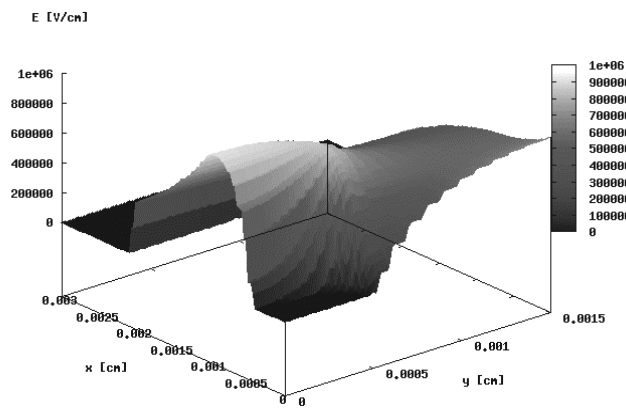

Figure 3: Electric field strength distribution at U_R=1000 V, device size 15 µm.

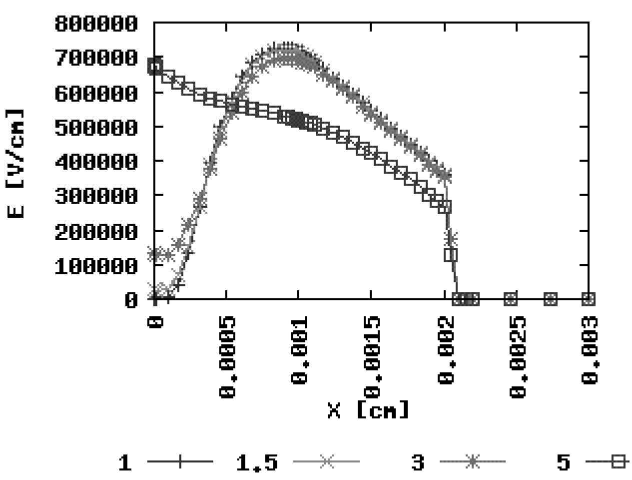

Figure 4: Electric field strength distribution dependence on device dimensions [µm].

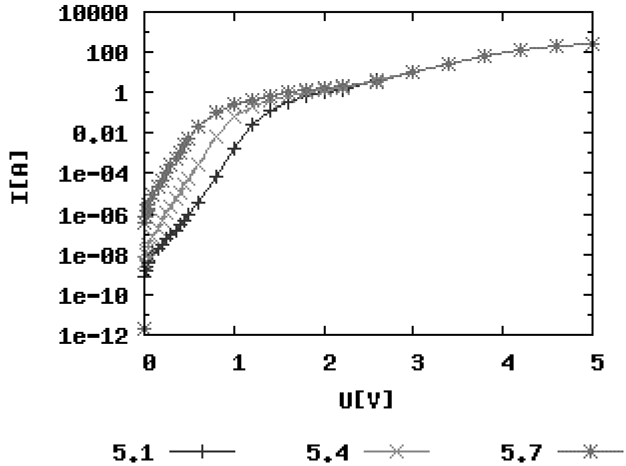

Figure 5: Forward characteristics dependence on contact metal work function [V] for *p*-substrate.

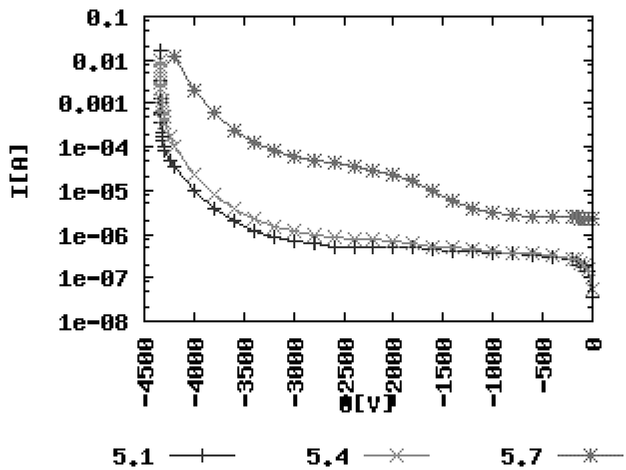

Figure 6: Reverse characteristics dependence on contact metal work function [V] for *p*-substrate.

The next analysis compares the Schottky JBS device with the pure *pn*- and Schottky diodes. Concluding from the working principles of JBS device the forward and reverse characteristics of JBS device are laying between the characteristics of pure Schottky diode and *pn*-diode, but on lower forward voltages values only Schottky part of the device conducts and on higher forward voltages only the *pn*-part of the device conducts. In case of reverse characteristics the breakdown voltage for *pn*-diode is lower compared to JBS device. The reason, why such a phenomenon takes place is that the dimension of the region, where the electric field strength is distributed is very narrow (only about 10 μm) and therefore the break down arrives earlier compared to classically possible situation. This statement is partly supported by the analysis of electric field strength distribution inside the device, where the electric field strength is distributed over a wider area than in case of *pn* diode, but its maximum value is still low and situated under surface. In switching processes the analysis of currents shows clearly that the Schottky part of the device acts against the *pn*-part of the device for a short period of time. Although eventually the turn-off time for Schottky structures is generally shorter than for *pn*-diode, it is important to stress that after as short as 30 ps the current of Schottky diode is already about 8 times smaller than of *pn*-diode, and 90% of reverse voltage is achieved already in 23 ns in case of Schottky diode. For the *pn*-diode this time period is about 600 ns.

Finally, we make some comments about the situation with *p*-substrate versus *n*-substrate. The forward current level for *n*-substrate device is about three orders of magnitude higher almost over the whole forward voltage region. The current values difference at low forward voltages is explained mostly by the lower barrier height of *n*-4H-SiC (about 1.1 eV) compared to *p*-4H-SiC (about 1.4 eV). We have to stress that the metal work function is taken to be the same for both cases. On higher forward voltages the majority of current flows through the *pn*-junction part of the device defining the current level differences for these situations. On reverse voltages the device with *n*-substrate has about two and a half orders of magnitude higher leakage current compared with the device with *p*-substrate. Similarly to the forward bias situation the low reverse voltage situation is also caused by the clear difference in barrier heights for *p* and *n*-type material (Schottky contact metal work functions have equal values for both cases).

The maximum value of the electric field strength is lower in case of *n*-substrate. The reason concludes from the slightly different dimensions of the width of the device's emitter region (in our simulations 1 μm for *p*-substrate JBS device). The turn-off time of *n*-substrate device is about 4 times higher compared to *p*-substrate device (Fig. 7). The reason for this significant difference stems directly from the differences of the values of holes and electron mobility's. For 4H-SiC the mobility of holes is almost 10 times lower than the mobility of electrons.

4 Conclusions

In this paper we have introduced some very new and original simulation results concerning JBS devices. First of all the parametric simulation for determining the best dimensioned device was discussed. After that the original results of *p*-substrate devices taking into account the Schottky contact metal work function and different SiC polytypes have been presented. There is still no *p*-substrate based JBS device examinations published. Finally, the comparison *p*-substrate versus *n*-substrate was presented. Our simulations revealed that *p*-substrate JBS devices have generally no substantial advantages over *n*-substrate devices, but in some particular categories we met strong advantages over *n*-substrate devices.

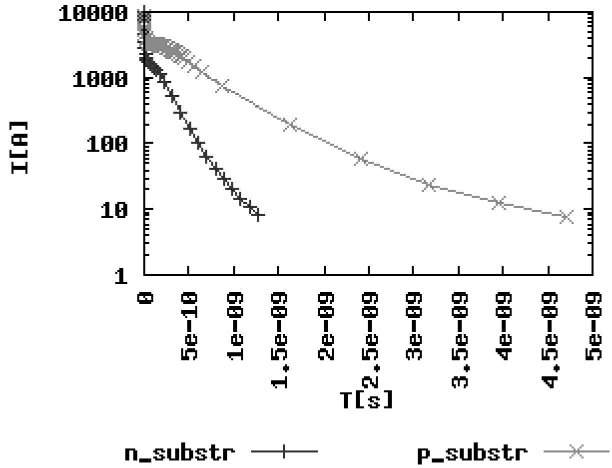

Figure 7: Turn-off time characteristics *n*- versus *p*-substrate.

The new findings we want to stress are the following:

- The deepness of *p*-region is the most important dimension in forming the shape of electrical field.
- Electrical field distribution is important in three aspects: maximum electric field strength determines avalanche breakdown of device, electric field strength under Schottky contact has influence on reverse current through Schottky barrier lowering, and the electrical field near the device surface has great importance on device surface breakdown phenomenon.

The dimensioning of the JBS devices results in the conclusion that there never exists the so called best device for all the conditions. The device has to be chosen keeping in mind mainly low-power losses in high power applications. It is an extremely important from the point of view of manufacturing technologies. The goal is to reduce or to keep the electric field strength under surface very low using the high quality and complex passivation solutions.

The model used in simulations does not include the description of the tunneling mechanisms. Tunneling can influence in particular situations the behavior of the device remarkably. Therefore additional investigation of JBS device behavior with inclusions of tunneling into the model would be an interesting subject for future investigations.

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