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Low temperature wafer bonding on silicon nitride

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Abstract

In the fabrication of micromachined devices, wafer bonding is an increasingly used technique for joining wafers. Most wafer bonding processes used today require firing temperatures above 800°C, which limits the use of this technique. For application in back-end processing, we developed a low temperature wafer bonding technique on LPCVD Si_3N_4 coated wafers. After firing bonded wafers at 250-350°C, the bonding strength was about 200erg/cm^2. However, the presence of gas bubbles at the bonded interface was observed. As a demonstrator application, a micromachined Si wafer containing membranes was bonded to a finished Si/Pyrex micromachined device wafer.

1 Introduction

Bonding at wafer scale is in many cases one of the last steps (before dicing) in the fabrication process of a micromachined sensor. This implies that high temperatures in this step are prohibited in order to avoid problems such as damage to Al metallisation. Several bonding techniques such as eutectic Au-Si (Wolffenbuttel[1]), low temperature Si-Si wafer fusion bonding (Tong[2]) or Pyrex-Si anodic bonding (Hannenborg[3]) can be used. However, bonding processes on Si_3N_4 have not been widely investigated (Ismail[4], Bower[5]), although Si_3N_4 layers are extensively used to make membranes, as KOH etching mask, or as passivation layer in micromachined devices.

In this paper, we report on the development of a technique for wafer bonding on Si_3N_4 layers at 250-350°C. After describing the experimental conditions, we analyse the bond strength on Si_3N_4 surfaces upon high temperature annealing. Next, we compare low temperature and high temperature bonding. Finally, we describe the application of this low temperature bonding on micromachined wafers.

2 Experimental conditions

A fusion bonding process consists of 4 steps: (a) cleaning cycle to remove particles; (b) surface pre-treatment to obtain the required surface condition, (c) pre-bond at room temperature, and (d) firing at elevated temperature for increasing the bond strength.

As a cleaning procedure, the wafers were cleaned by a sequence used in our lab for CMOS processes. The cleaning consists of H_2SO_4:H_2O_2 (4:1) for 10 min, H_2O/HF(0.5%) for 2 min, and 20 min of DI rinse after each step. Next, the wafer surface was made hydrophilic by exposing it to H_2SO_4:H_2O_2 (4:1) for 10 min followed by 20 min of DI rinse. The prebonding was done in a commercially available (Electronic Vision) alignment system. This system bows one of the wafers before bringing them into contact. Therefore, the bonding starts from the centre of the wafer and expands to the substrate's border, thus avoiding the trapping of air bubbles at their interface. Finally, the wafer pair was annealed in a N_2 ambient.

Scanning Acoustical Microscopy (SAM) (Moore[6]) was used to obtain information on the bonded interface. In comparison to the more widely used IR transmission spectroscopy method, we found that SAM allowed to resolve the presence of much smaller defects at the interface, and therefore was the preferred method of analysis. The method was used for qualitative measurements of defect densities, as well as to calculate the surface energy of the bond (Fig. 1). In this method to calculate the surface energy of the bond (Maszara[7]), a blade is inserted at the bonded interface. This separates the wafers over a length L, which is related to the surface energy of the bond by the formula shown in figure 1. In this expression, E and t are the modulus of elasticity and thickness of the Si wafer respectively, 2y is the thickness of the blade and L is the crack length.

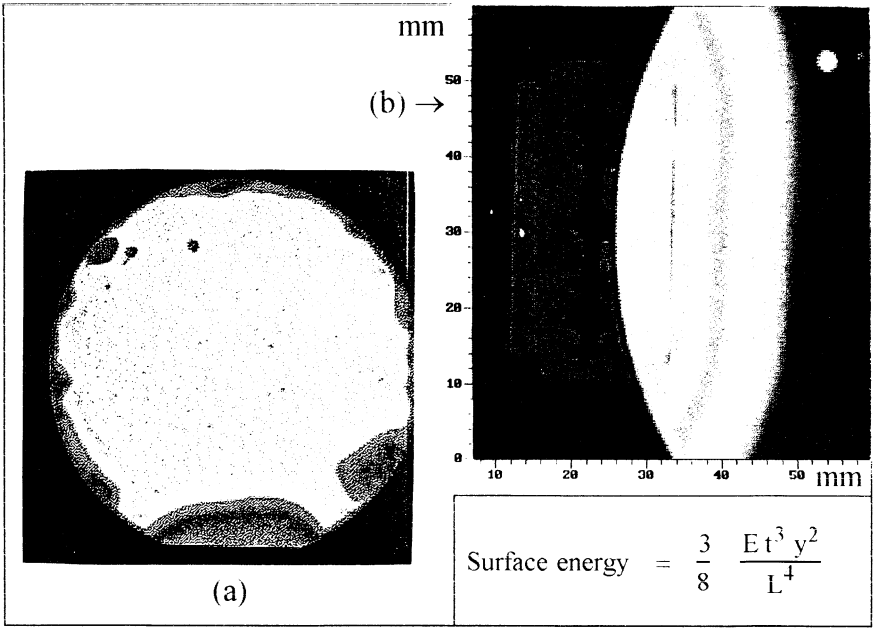

Figure 1: Typical SAM pictures of wafers with SiO_2(320nm)/Si_3N_4 (100nm) coating which were fusion bonded and annealed at 250°C, 3h in N_2. (a) Top view of a badly bonded 5 inch wafer with several inclusions visible as dark areas. (b) Measurement of the surface energy: a razor blade is inserted at the interface and separates the wafers over a length L.

3 High temperature wafer fusion bonding on Si_3N_4

Stoechiometric LPCVD Si_3N_4 was chosen since it is extensively used in micromachined devices as KOH etching mask, or as passivation layer or even to make membranes. Since LPCVD Si_3N_4 layers are stressed (Sze[8]), we firstly studied the influence of the stress on the surface energy of the bonding.

We chose to control the net stress in the wafer by means of stress compensation of the Si_3N_4 by a SiO_2 layer which is first deposited on the wafer. Since the stress is tensile in Si_3N_4 films and compressive in SiO_2 films (Sze[8]), the net stress can be made equal to zero.

To detect any influence of stress on the surface energy of the bonding, the relation between both was evaluated under a typical and standard high temperature bonding experimental condition: 800°C, 2h in N_2 (Harendt[9]).

Figure 2 shows the relation between thickness of the SiO_2 layer and the net stress in the film. Figure 3 shows the corresponding surface energy.

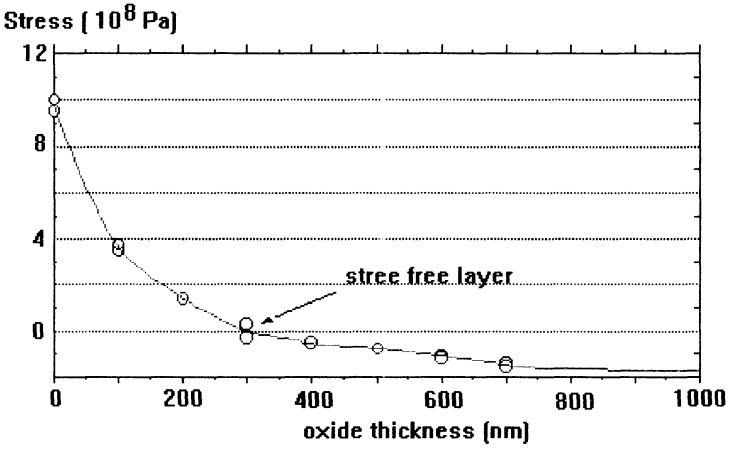

Figure 2: Total stress in the SiO_2/Si_3N_4 stacked layer versus thickness of SiO_2.

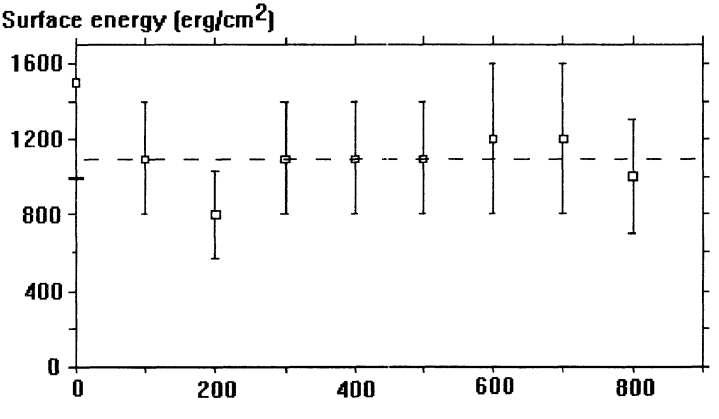

Figure 3: Surface energy of the bond for bonding at 800°C/3h/N_2.

From figure 3 we see that there is not a significant influence of stress on the surface energy of the bond, except for wafers without any oxide. We also observe that the surface energy has a mean value of (1100±200)erg/cm^2, which is in agreement with the value reported by literature (1000±100)erg/cm^2 (Harendt[9]).

This result confirms that in our experimental set-up, although the stress can make the bonding more difficult (bowing the wafer), it does not

affect the final surface energy of the bonding which is only determined by the bonded material and the experimental conditions for the annealing (Tong[2]).

4 Low temperature wafer fusion bonding on Si_3N_4

Since we were interested to apply our technique to Si_3N_4 layers used in sensitive membranes, where it is important to work with stress free layers, we chose stress free wafers (SiO_2/Si_3N_4 layers with 320/100nm) for the further experiments. Figure 4 shows the surface energy of the bond as a function of the annealing temperature.

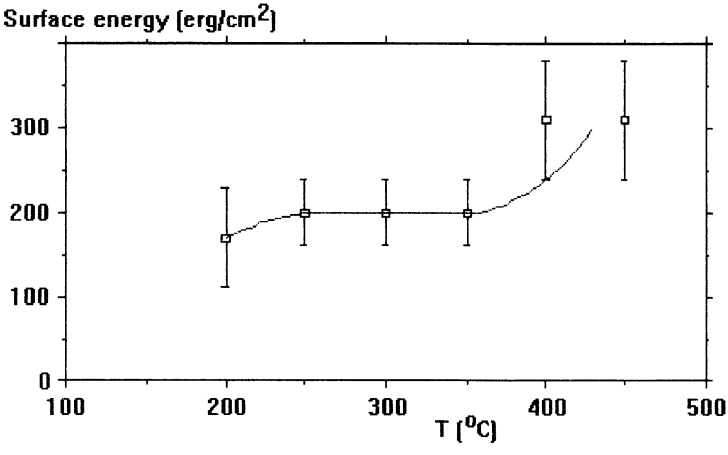

Figure 4: Surface energy of bond versus temperature of annealing. Annealing time of 3h.

Figure 4 shows that the surface energy of the bonding has a value of (190±20) erg/cm^2 at 250-350°C, which increases for higher temperatures. A similar relation between surface energy and temperature of annealing is observed in Si-Si bonding in this temperature range (Tong[2]). We also report that experiments performed for 100h of annealing showed similar results and the surface energy did not show a significant increase, (230±60)erg/cm^2.

To evaluate the quality of the bond, samples annealed at 300°C were diced into 2x2mm^2 squares, which were subsequently subjected to a 15min ultrasound treatment in water at room temperature (Peeters[10]). The percentage of separated diced pieces was 2%, which demonstrates the absence of major defects at the interface. On a smaller scale however, we

always observed defects, attributed to gas bubbles, at the bonded interface (figure 1).

These bubbles have been observed for Si bonding at low temperature and are reported by several authors (Tong[2],Maszara[11]-Mitani[13]] to be caused by H_2 (released during decomposition of water trapped on the wafers' surface during the hydrophilation process), or, alternatively, attributed to outgassing of hydrocarbons present at the wafers' surface. Since stringent wet cleaning and clean-room conditions were used in our experiments, we believe that the gas bubbles observed in our experiments may be identified as H_2 bubbles.

In this case there are three solutions reported for Si to eliminate or at least reduce these bubbles: (a) thermal annealing 30min at 600°C in O_2 before the bonding (Tong[2]); (b) annealing in N_2 at temperatures higher than 700°C after the bonding (Harendt[9], Bengtsson[12]]; (c) immersing the samples in boiling H_2NO_3 for at least 1h before the bonding (Peeters[10]).

Since we are interested in low temperature processes, we considered only the alternative c (immersing the samples in boiling H_2NO_3). However, we confirmed that this procedure that works for Si did not work properly in our experiments with Si_3N_4.

Yamaguchi[14] reports another solution to reduce this problem. This consists in making sacrificial trenches on the surface to be bonded. In this case, using a proper design and distribution of these trenches, it is possible to trap most of the gas bubbles.

5 Process design of micromachined devices for low temperature bonding on Si_3N_4

A micromachined IR detector based on the principle of a pneumatic cell and suited as an IR detector was presented by Chévrier[15] as an example showing the potential of the bonding technique on Si_3N_4 presented in this paper. Figure 5 shows a cross section of the detector.

It consists basically of a sealed cavity, in which the heat generated by absorbed IR light results in an increased gas pressure. This pressure rise is detected capacitively. At the wafer-assembling process step, the device could not be submitted to temperature higher than 500°C. Thus, the two silicon wafers were bonded using the technique described in this paper. The bottom wafer was coated with thermal SiO_2 and LPCVD Si_3N_4. A pneumatic leak between the sealed cavity and the capacitor was necessary to balance the over-pressure between the two sides of the membrane due to temperature. Measurements of the response time of this pneumatic leak

have shown a sufficient sealing quality of the bonding (see the detail in Chévrier[15]) for this application.

Concerning the H_2 bubbles discussed in the previous chapter, the cavities in this sensor have the same effect as "sacrificial" trenches i.e., they trap most of the H_2 bubbles. Anyway, it is convenient to make a proper design of "sacrificial" trenches in order to reduce the problem with bubbles to an acceptable level.

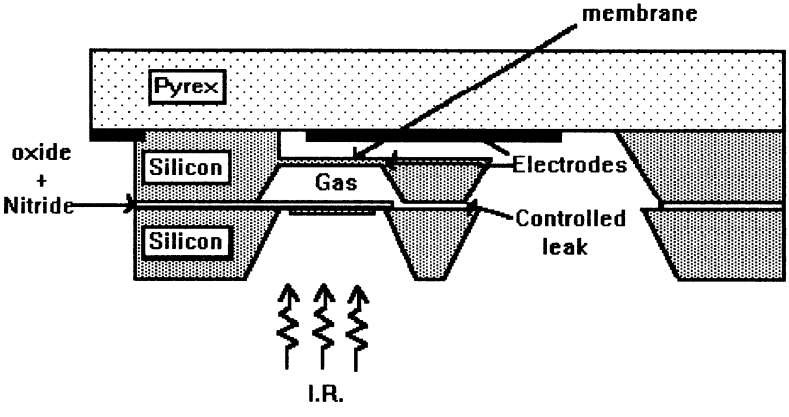

Figure 5: Cross section of the experimental Golay cell developed by Chevrier[15].

6 Conclusions

Wafer fusion bonding on nitride layers is possible under low temperature firing conditions and presents acceptable values for surface energy (200 erg/cm^2 for 300°C annealing). The annealing temperature is compatible with any IC process and was applied to a demonstrator device resulting in operational devices. A proper design of "sacrificial" trenches reduce the problems with gas bubbles to an acceptable level.

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