



Duality of transmission line models for circuit simulation

K.K. Fung,^a S.Y.R. Hui^b

^aSchool of Electrical Engineering, University of Technology, Sydney, New South Wales 2007, Australia

^bDepartment of Electrical Engineering, University of Sydney, New South Wales 2006, Australia

Abstract

This paper discusses Norton transmission line (TL) link models for the simulation of reactive circuit components. These models follow the traditional Thevenin transmission line modelling (TLM) approach and retain the obvious physical concepts of the TL models. However the proposed Norton models allow nodal analysis technique to be used, overcoming the inherent difficulties in system matrix formation using the Thevenin models. In this paper, the Norton models are derived from the Thevenin models and validated by the simulation of a high frequency switch mode power supply circuit. Details of the simulation process are discussed step by step in a tutorial style.

1 Introduction

The TLM method was first used by Johns to solve field problems in the early seventies (Johns[1]). It has since been developed and generalised to solve circuit problems. There are two basic modelling units in TLM, namely the stub and the link. TL stub models were one-port models introduced to simulate circuit components, such as capacitors, inductors, mutual inductances, diodes and switches (Hui[2,3]). Link models were proposed as two-port models and are particularly useful for the simulation of stiff reactive components and isolating non-linear components from the remaining linear circuits. Link models decouple complex electric circuits into smaller sub-circuits, allowing simpler formulation of circuit equations and opening up the possibilities of parallel simulation (Hui[4], Fung[5]). Because all these traditional TL models are based on the Thevenin equivalent circuits, they restrict users to mesh analysis, which is not always desirable. In a given circuit, mesh loops can be selected in different ways.

106 Software for Electrical Engineering

This variation leads to difficulties in automating system equations formulation. For computer aided circuit analysis, the nodal approach is usually preferred. It allows easy, unambiguous formulation of circuit equations since the number of nodes are fixed.

2 Thevenin transmission line models

The Thevenin stub and link models used to simulate reactive components are briefly summarised below. Further details can be found in reference 2 to 5.

Consider a capacitor C with voltage nV_c and current nI_c shown in Fig. 1a. A capacitor can be modelled as a TL stub with an open circuit termination, as shown in Fig. 1b, where Z_c is the characteristic impedance, nV_c^i is the incident voltage and nV_c^r is the reflected voltage at time step n . Inside the transmission line, it takes one time step T for a voltage pulse to travel from the left end to the termination and then reflected back to the left end. The open circuit termination means that a capacitor has a reflection coefficient of $+1$. The characteristic impedance Z_c is $T/2C$ where C is the capacitance in Farads. The Thevenin stub model for the capacitor is shown in Fig. 1c.

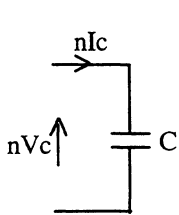


Fig. 1a Capacitor

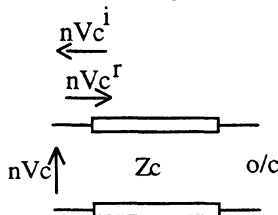


Fig. 1b TL stub

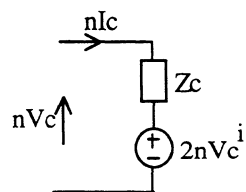


Fig. 1c Thevenin model

Similarly an inductor L shown in Fig. 2a can be modelled as a transmission line stub with a short circuit termination as shown in Fig. 2b. Due to the short circuit, an inductor stub has a reflective coefficient of -1 . It can be shown that the characteristic impedance is $2L/T$. Fig. 2c shows the Thevenin stub model for the inductor.

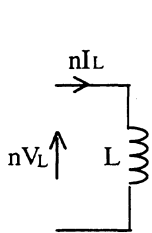


Fig. 2a Inductor

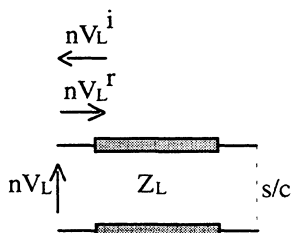


Fig. 2b TL stub

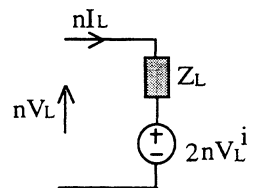


Fig. 2c Thevenin model

Link models can be employed to simulate stiff reactive components often found in power electronic circuits. Fig. 3a shows a capacitor that links two sub-circuits with end voltages nV_{ca} and nV_{cb} . This 'linking capacitor' can be considered as a transmission line link as shown in Fig. 3b, where at time step n , the incident voltage on side a is nV_{ca}^i , the reflected voltage is nV_{ca}^r ; the corresponding incident voltage on side b is nV_{cb}^i and the reflected voltage is nV_{cb}^r . It takes one time step T for a voltage pulse to travel from one end of the model to the other. The transmission line characteristic impedance Z_c is equal to T/C . Fig. 3c shows the Thevenin link model for the capacitor.

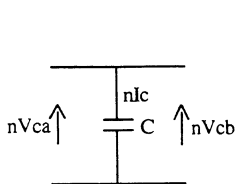


Fig. 3a Capacitor

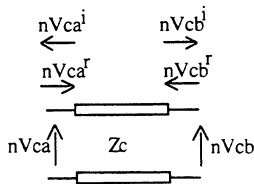


Fig. 3b TL link

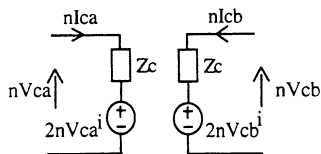


Fig. 3c Thevenin model

Similarly an inductor that links two sub-circuits shown in Fig. 4a can be modelled by a transmission line shown in Fig. 4b with the respective incident and reflected voltages. The characteristic impedance Z_L of the transmission line is L/T . Fig. 4c shows the Thevenin link model for the inductor.

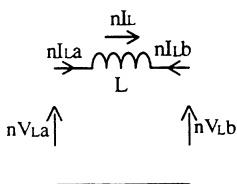


Fig. 4a Inductor

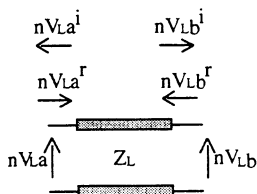


Fig. 4b TL link

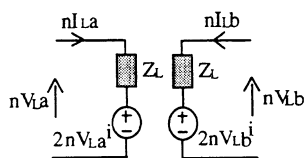


Fig. 4c Thevenin model

3 Norton transmission line models

3.1 Capacitor stub

If a capacitor is modelled by a transmission line stub in which the incident and reflected currents are considered instead of incident and reflected voltages, Norton TL models can be derived. It can be seen from Fig. 5a and Fig. 5b that at time step n , the following relationship exists between the voltages and the currents travelling within the transmission line.

$$nI_c^i = nV_c^i / Z_c \quad (1)$$

108 Software for Electrical Engineering

$$nIc^r = nVc^r/Zc \quad (2)$$

In Fig. 5b, nIc^i interacts with the rest of the circuit to produce a reflected current nIc^r . Applying Kirchoff's current law,

$$nIc^r = nIc + nIc^i \quad (3)$$

The reflected current nIc^r travels towards the termination end. Since the termination is open circuit, the reflection coefficient is +1 and therefore Ic^r equals Ic^i . This new reflected current Ic^r then travels back to become the new incident current at the beginning of the next time step $n+1$. The length of the TL stub is so chosen that it takes one time step T for a current or voltage pulse to make a round trip. Assuming the transmission line is lossless,

$$n+1Ic^i = nI^r \quad (4)$$

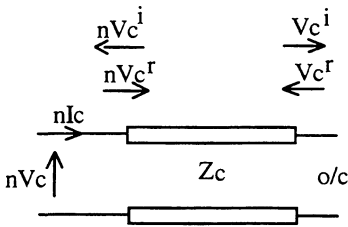


Fig. 5a Conventional TL stub

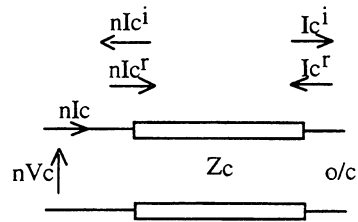


Fig. 5b Norton TL stub

Using simple circuit analysis, the capacitor Thevenin stub model shown in Fig. 6a can be converted to an equivalent Norton form as shown in Fig 6b. Applying equation (1) then gives the Norton model shown in Fig. 6c. It consists of a current source connected in parallel with the input admittance Yc of the capacitor, where Yc equals $1/Zc$. The magnitude of the current source is equal to twice the incident current nIc^i at time step n .

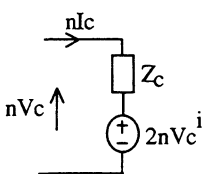


Fig. 6a Thevenin

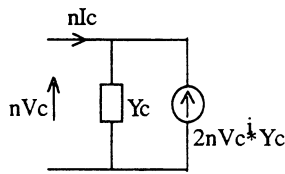


Fig. 6b Norton form

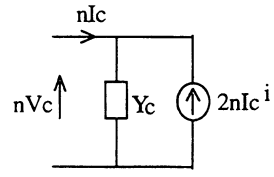


Fig. 6c Norton model

3.2 Inductor stub

An inductor shown in Fig. 7a can be considered as a transmission line stub with a shorted termination as shown in Fig. 7b. The proposed Norton TL model is

shown in Fig. 7c. The value of the input admittance Y_L is $T/2L$. Because of its short circuit termination the transmission line stub has a reflection coefficient of -1 . To conform to standard convention, the current source is downwards.

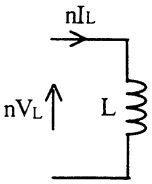


Fig. 7a Inductor

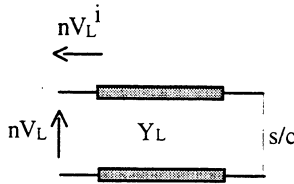


Fig. 7b TL stub

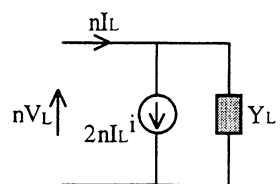


Fig. 7c Norton model

3.3 Capacitor link model

The Norton TL link model for a link capacitor is shown in Fig. 8c. The characteristic admittance Y_c for the link model is equal to C/T , where C is the capacitance and T is the time step chosen. It takes one time step for a current pulse to travel from one end of the TL section to the other.

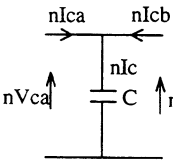


Fig. 8a Capacitor

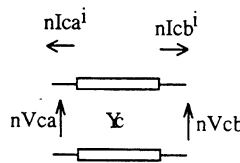


Fig. 8b TL link

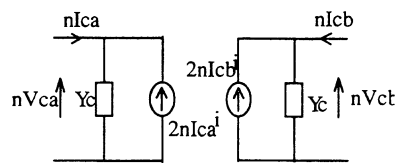


Fig. 8c Norton model

3.4 Inductor link model

Similarly, a smoothing inductor used in a circuit to filter out current ripples can be regarded as an inductor link shown in Fig. 9a. The equivalent transmission line link can be found in Fig. 9b. The Norton TL model is shown in Fig. 9c. This inductor link model is again similar to the capacitor link model. The only difference lies in the input admittance Y_L which is equal to T/L .

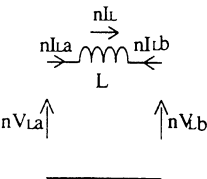


Fig. 9a Inductor

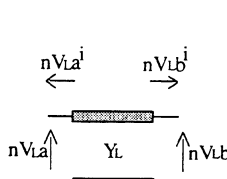


Fig. 9b TL link

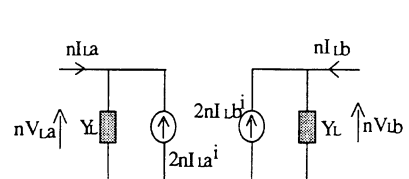


Fig. 9c Norton model

110 Software for Electrical Engineering

4 Circuit Simulation

As an example, the Norton models proposed were used to simulate a switched power supply fed by a capacitively smoothed rectifier circuit as shown in Fig. 10. For illustration purposes, it was decided to simulate the source inductance L_s , inductor L and capacitor C_2 as TL stubs, and C_1 as a TL link. Inductor L has to be simulated as a stub because it is connected in parallel and consequently does not 'link' the two sides. For simplicity, diodes and switch are simulated as switched resistances. When the switch or diode is conducting, it is represented by a resistance of 1Ω . Otherwise it is modelled as a $10 \text{ K}\Omega$ resistor. The equivalent circuit for the switched power supply can be found in Fig. 11 where the four reactive components are marked in dotted boxes. The ac source V_s and internal resistance R_s are replaced by a current source $V_s * G_s$, shunted by an equivalent source conductance G_s .

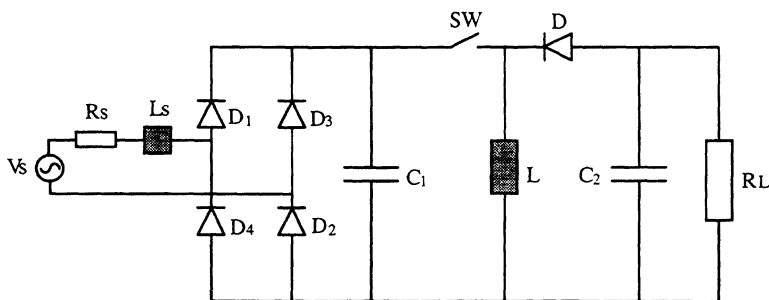


Fig. 10 High Frequency Switch Mode Power Supply Circuit

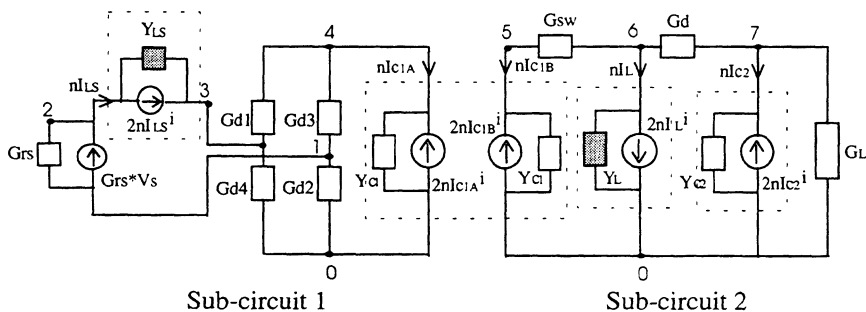


Fig. 11 Equivalent circuit using Norton TL models

Altogether 8 nodes can be identified. Take node 0 as reference, the voltages at nodes 1 to 7 can be found by nodal analysis. Apply Ohm's law to each sub-circuit.

$$\begin{bmatrix} \text{Grs}+\text{Gd2}+\text{Gd3} & -\text{Grs} & 0 & -\text{Gd3} \\ -\text{Grs} & \text{Grs}+\text{YLS} & -\text{YLS} & 0 \\ 0 & -\text{YLS} & \text{YLS}+\text{Gd1}+\text{Gd4} & -\text{Gd1} \\ -\text{Gd3} & 0 & -\text{Gd1} & \text{Gd1}+\text{Gd3}+\text{Yc1} \end{bmatrix} \begin{bmatrix} \text{V1} \\ \text{V2} \\ \text{V3} \\ \text{V4} \end{bmatrix} = \begin{bmatrix} -\text{Grs}*\text{Vs} \\ (\text{Grs}*\text{Vs} \\ -2*\text{nILs}^i) \\ 2*\text{nILs}^i \\ 2*\text{nIc1A}^i \end{bmatrix}$$

$$\begin{bmatrix} \text{Yc1}+\text{Gsw} & -\text{Gsw} & 0 \\ -\text{Gsw} & \text{Gsw}+\text{Gd}+\text{YL} & -\text{Gd} \\ 0 & -\text{Gd} & \text{Gd}+\text{Yc2}+\text{GL} \end{bmatrix} \begin{bmatrix} \text{V5} \\ \text{V6} \\ \text{V7} \end{bmatrix} = \begin{bmatrix} 2*\text{nIc1B}^i \\ -2*\text{nIL}^i \\ 2*\text{nIc2}^i \end{bmatrix}$$

Next all the model currents can be found by applying Kirchoff's current law,

$$\text{nILs} = (\text{V2}-\text{V3})*\text{YLS}+2*\text{nILs}^i$$

$$\text{nIL} = \text{V6}*\text{YL}+2*\text{nIL}^i$$

$$\text{nIc2} = \text{V7}*\text{Yc2}-2*\text{nIc2}^i$$

For capacitor C₁,

$$\text{nIc1A} = \text{V4}*\text{Yc1}-2*\text{nIc1A}^i$$

$$\text{nIc1B} = \text{V5}*\text{Yc1}-2*\text{nIc1B}^i$$

By applying equation (3) and taking into account the reflection coefficients, the reflected currents at the end of time step n can be found. These become the incident currents at the beginning of the next time step.

$$\text{n+1ILs}^i = \text{nILs} - \text{nILs}^i$$

$$\text{n+1IL}^i = \text{nIL} - \text{nIL}^i$$

$$\text{n+1Ic2}^i = \text{nIc2} + \text{nIc2}^i$$

Since capacitor C₁ is modelled as a two port link, the reflected currents on side A is (nIcA+nIcAⁱ) and the reflected current on side B is (nIcB+nIcBⁱ). These currents travel towards the opposite sides to become the incident currents at the next time step. The transmission coefficient is +1.

$$\text{n+1IcA}^i = \text{nIc1B} + \text{nIc1B}^i$$

112 Software for Electrical Engineering

$$n+1I_{C1B}^i = nI_{C1A} + nI_{C1A}^i$$

Since all incident currents at the beginning of the next time step are now known, all current sources in the next time step in Fig. 11 are known. The above procedure can proceed from one time step to the next.

Simulation was carried out for ten 50-Hz mains cycles using a time step of 1 μ sec. The simulated wave forms of the steady state voltages and currents are shown in Fig. 12 and 13. For generality, all initial incident currents are assumed to be zero, though estimated initial values may yield outputs faster.

Circuit parameters used are:

Mains 42 volts at 50 Hz

Switching frequency at 25 KHz and duty cycle of 0.34

Diode on resistance = 1.2 Ω

Diode off resistance = 10 K Ω

Switch on resistance = 1 Ω

Switch off resistance = 10 K Ω

Source resistance R_s = 1 Ω

Load resistance R_L = 23 Ω

Source inductance L_s = 5 μ H

Inductance L = 630 μ H

Capacitor C_1 = 1000 μ F

Capacitor C_2 = 100 μ F

Measured results are shown in Fig. 14 and 15. It can be seen that simulation and measurement agree well with each other, thus confirming the validity of the Norton TL models.

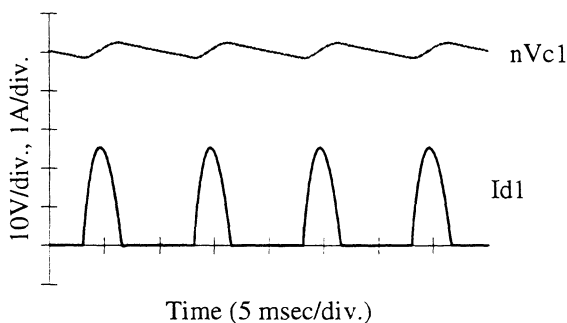


Fig. 12 Simulated capacitor voltage of C_1 and output current of rectifier i_3

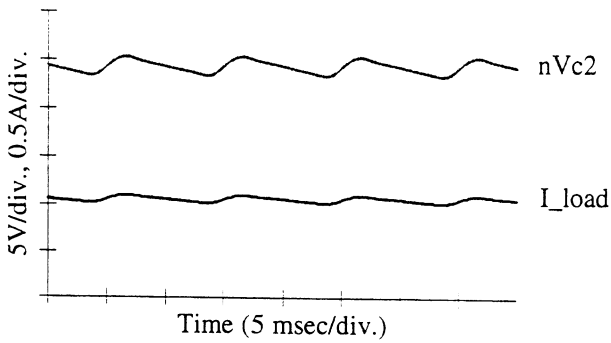
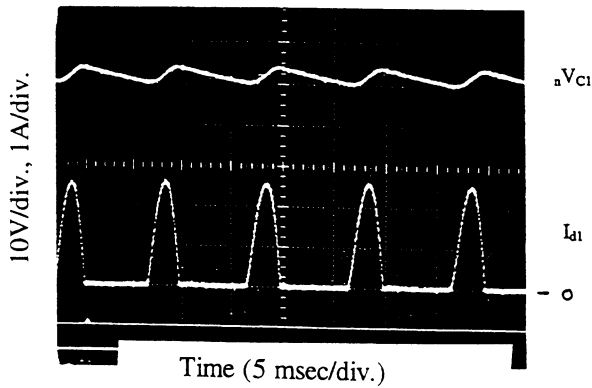
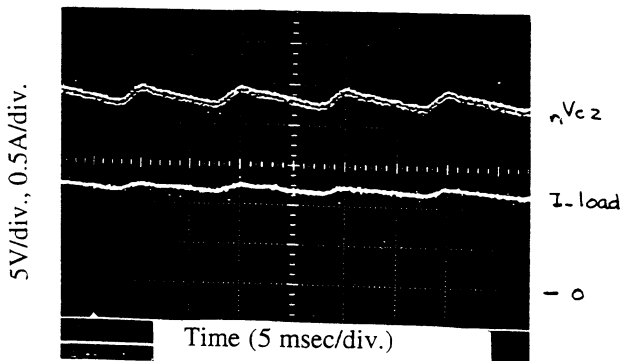
Fig. 13 Simulated voltage of C2 and I_{load} 

Fig. 14 Measured capacitor voltage of C1 and output current of rectifier i3

Fig. 15 Measured voltage of C2 and I_{load}



114 Software for Electrical Engineering

5 Conclusion

Norton TL stub and link models for reactive components are introduced. Previous models were based on Thevenin equivalent circuits, which use the concepts of incident and reflected voltages. Although the Norton models are complementary to the Thevenin models, their operations are based on incident and reflected currents. These models retain the obvious physical characteristics of the Thevenin TL models, yet allowing nodal analysis to be carried out using the transmission line technique, making it easier to formulate system equations automatically.

References

1. Peter B. Johns, Mark O'Brien, Use of the transmission-line modelling (t.l.m.) method to solve non-linear lumped networks, *The Radio and Electronic Engineer*, January/February 1980, Vol.50, No. 1/2, pp. 59-70
2. S.Y.R. Hui and C. Christopoulos, Numerical simulation of power circuits using transmission line modelling, *IEE Proceedings*, November 1990, Vol. 137, Pt. A, No. 6
3. S.Y.R Hui and C. Christopoulos, Computer Simulation of a Converter-Fed DC Drive Using the Transmission-Line Modeling Technique, *IEEE Transactions on Power Electronics*, Oct. 1991, Vol. 6, No.4
4. S.Y.R Hui, K.K. Fung and C. Christopoulos, Decoupled Simulation of DC-Linked Power Electronic Systems Using Transmission-Line Links, *IEEE Transactions on Power Electronics*, January 1994, Vol. 9, No.1
5. K.K. Fung, S.Y.R. Hui, C. Christopoulos, Parallel Simulation of Electrical Circuits using the TLM Technique, *Electrosoft 93*, Software Applications in Electrical Eng, Southampton U.K., July 1993, pp. 21-28