



Expert system issues related to monolithic microwave integrated circuit design

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ABSTRACT

Artificial Intelligence (AI) techniques are applied to develop a framework for the design and layout of MMIC circuits. This framework addresses key aspects of the design process, from circuit specification and initial design decisions through to final layout and preparation of the circuit for fabrication. A number of knowledge-based systems are incorporated into the framework to assist in specific design areas, with amplifier design chosen to demonstrate the principles employed.

INTRODUCTION

Monolithic Microwave Integrated Circuits (MMICs), which are essentially microwave ASICs, are emerging as key elements in high frequency electronic systems. They are ideal where high speeds and miniature size are required and are finding applications in cellular radio, domestic satellite television receivers, and in radar and collision avoidance systems.

MMICs are integrated circuits fabricated on Gallium Arsenide (GaAs) requiring an intricate fabrication process which is performed by specialist design foundries. Within the United Kingdom GEC-Marconi Materials Technology Ltd [1] provide the sole foundry service, offering a 20GHz process using FETs as the active device, and recently introducing a 35GHz HEMT based process.

The design of MMICs is a complex task, requiring considerable skills and experience on the part of the microwave engineer. Apart from



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traditional microwave circuit design techniques, the engineer must be familiar with the foundry process used. GEC-Marconi outline a recommended procedure for the MMIC process [2]. The principal stages in the design are outlined below.

Circuit Specification A formal specification is required for the circuit, detailing the technical requirements such as frequency of operation and bandwidth.

Initial Design Selections The circuit topology to be used for the design must be chosen. For example, if the specification is for a broadband amplifier a choice must be made between reactive, feedback or distributed circuits. Each element of the specification will place some constraint on the topology which would be suitable, and the designer normally bases this decision on previous experience. At this stage in the design an active device (FET, HEMT) must also be identified. Often, a number of topologies and devices are chosen, and initial circuit design carried out to find the optimum.

Circuit Design Based on the above design decisions, an initial design is carried out for the circuit. This is performed with the aid of commercial circuit simulators such as Harmonica™ or Touchstone™. These simulators incorporate optimisation routines which are also used at this stage of the design. It is important that the circuit more than meets the specification at this stage of the design since parasitics will later be introduced which will degrade the circuit's performance.

Sensitivity Analysis It is critical in any design to ensure that the variation of specific components within their tolerance bands does not cause the circuit to go out of specification. Sensitivity analysis should be carried out by varying values of components across their tolerance range as quoted by the foundry process. Again, commercial circuit simulators support sensitivity analysis.

Inclusion of Parasitics Monolithic circuit elements have complex equivalent circuit models, which are defined by the foundry process. Figure 1 shows the GEC-Marconi model for their spiral inductor. The effect of such parasitics can considerably degrade the circuit performance, and must be included in the design. Each prime element of the ideal design is converted to its electrical equivalent circuit, and the resulting circuit re-optimised to meet the specification. If this is not possible, then the circuit is discarded and a new topology and/or FET chosen. Inclusion of parasitics is seen as a critical aspect since a *right first time* design is required for monolithic circuits. MMIC technology is therefore design



intensive, resulting in high non-recurrent engineering (NRE) costs. Unlike hybrid circuits, there is no opportunity to alter a component after fabrication.

Circuit Layout The final task in the MMIC design cycle is layout of the circuit. The close proximity of elements on the MMIC chip can lead to extensive inter-component coupling. Again, the foundry in use supplies a set of rules which must be adhered to by the designer. These cover aspects such as the minimum spacing between components.

The overall MMIC design cycle is therefore complex and requires an in-depth knowledge of the specific foundry process. It has been noted that recent advances in MMIC technology have not been accompanied by the necessary advances in design expertise. This has resulted in a shortage of skilled MMIC designers, and the design framework under development redresses this problem, deskilling the foundry-user interface and offering a training environment for the inexperienced engineer.

MMIC DESIGN FRAMEWORK

Figure 2 shows the overall structure of the MMIC design framework [3]. The structure relates directly to the stages of the MMIC design process described in the previous section. To demonstrate the principles involved, the specific application of amplifier design is considered. However, this could be extended to cover other aspects such as oscillator or filter design.

Viewing the framework from the top-level, at section I the designer enters the circuit specification, which, for the case of the amplifier, includes the gain, bandwidth, noise figure and VSWR requirements. Control passes to an initial expert system which selects an optimum topology and FET for the circuit. This system is discussed in the following section. Design of the ideal circuit schematic is addressed in part II of the framework, which includes links to Super Compact™ for circuit simulation and sensitivity analysis. On completion of this section, an ideal circuit schematic is produced which satisfies the requirements specification.

Control then passes to section III of the framework where a second expert system GALEDA (also described below), converts each ideal circuit element to its equivalent electrical circuit, and maintains a library of the circuit cells. As each component is modified the circuit is re-optimised to meet the original specification. When complete, the circuit is ready for layout.



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EXPERT SYSTEM FOR AMPLIFIER TOPOLOGY AND FET SELECTION

An expert system is essentially the computer simulation of the behaviour of an expert within a specific domain. In the selection of topology and FET for an amplifier, the designer uses a combination of previous experience and rules of thumb to make the correct choices. The overall structure of the expert system is shown in figure 3. All rules of thumb and heuristics used by the expert are incorporated into the knowledge base, which is then processed by the inference engine.

Formulation of the knowledge base is the main consideration in developing an expert system. Rules of thumb relating to the suitability of each topology are identified. For example, it is known that the reactive circuit is limited to bandwidths of less than 20%. Above this bandwidth a feedback or possibly distributed topology is preferred. S-parameter data and FET models for devices available under the foundry process are stored in a database which is accessed and used by closed form expressions when investigating the suitability of a particular FET.

The expert system is developed using the Prolog programming language, used in a windowing environment on PC [4]. Operation of the system is demonstrated using a specified gain of 5dB and bandwidth of 2-16GHz. Due to the multi-octave bandwidth, the distributed amplifier is inferred as the optimum. The distributed amplifier [5], as shown in figure 4, is formed by cascading a number of FETs in such a way that their transconductance is combined without paralleling their input and output capacitances. Decade bandwidths have been reported for the distributed amplifier with the upper frequency limit constrained by the FET's input capacitance. For the present specification 3 devices are selected, the optimum being a 2 fingered device with a 100 μ m finger width. Under the GEC-Marconi process 2, 4 and 6 fingered devices are available, each with variable finger width from 50 μ m to 175 μ m. The system predicts that 4 FETs are required to meet the gain specification, and figure 5 compares the response predicted by the expert system with that obtained from a simulation using Super Compact. It can be seen that the two agree closely and the chosen FET meets both the gain and bandwidth specifications.

GALLIUM ARSENIDE LUMPED ELEMENT DESIGN ASSISTANT (GALEDA)

GALEDA [6,7] is the second expert system based program which is incorporated into the design framework. This system, which has a similar structure to the previous systems, contains a knowledge base, inference



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engine and user interface. As introduced previously, GALEDA converts each ideal element of the circuit schematic to its equivalent electrical model. This involves choice of the geometrical structure for each component, either from standard foundry library components or using a custom cell.

Key aspects of GALEDA include the use of 'beam' search techniques using relaxation, heuristics and caching. The number of possible solutions to a typical question, for example 'what are the physical dimensions of a component required to give 50Ω resistance?', can be of the order of 32×10^6 .

GALEDA also includes more conventional facilities such as calculator routines and manual search capabilities, allowing the user to 'zoom in' on particular domain areas. Basic explanation facilities are also provided. At present GALEDA contains about 90% of the design information supplied by the foundry, that is, the required information directly applicable to specific component design and layout.

CIRCUIT LAYOUT

The last phase in MMIC design is production of a fabrication mask for the foundry process. This involves placement of the component cells produced by GALEDA. Usually, the aim in MMIC design is to minimise real estate usage to reduce cost and increase yield. This results in increased coupling between component cells which degrades circuit performance. Although the foundry process provides rules for layout, designers will invariably develop their own rules of thumb through experience. The last stage of the design framework is the production of a knowledge-based system to assist in the layout process. Electromagnetic simulators such as Explorer™ or Sonnet™ will be used to assist in rules generation and layout modelling.

CONCLUSIONS

An "intelligent" design framework has been described which automates the MMIC design process. The framework supervises the overall design strategy used by the MMIC designer, calling on knowledge-based sub-systems to advise on specific areas of the design such as choice of optimum topology and FET for the circuit specification and addition of foundry dependent parasitics. Commercial design tools are also incorporated for procedural aspects of the design such as simulation and layout. The framework concentrates on design of MMIC amplifiers using the GEC-Marconi foundry process. However, this could be developed to cover other



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applications such as oscillator or filter design, and other device foundries.

Research is now concentrating on automating layout of the MMIC chip, using the rules of thumb for layout supplied by the foundry. Completion of this stage will yield a comprehensive design framework, enabling engineers without specific foundry experience to take advantage of MMIC technology.

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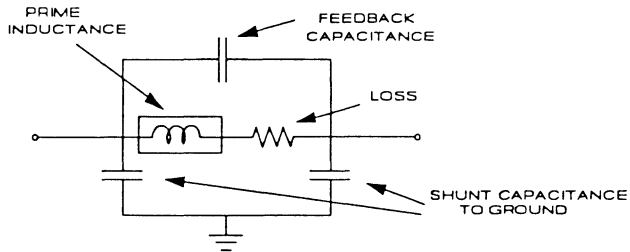


Figure 1 : Parasitics of Spiral Inductor

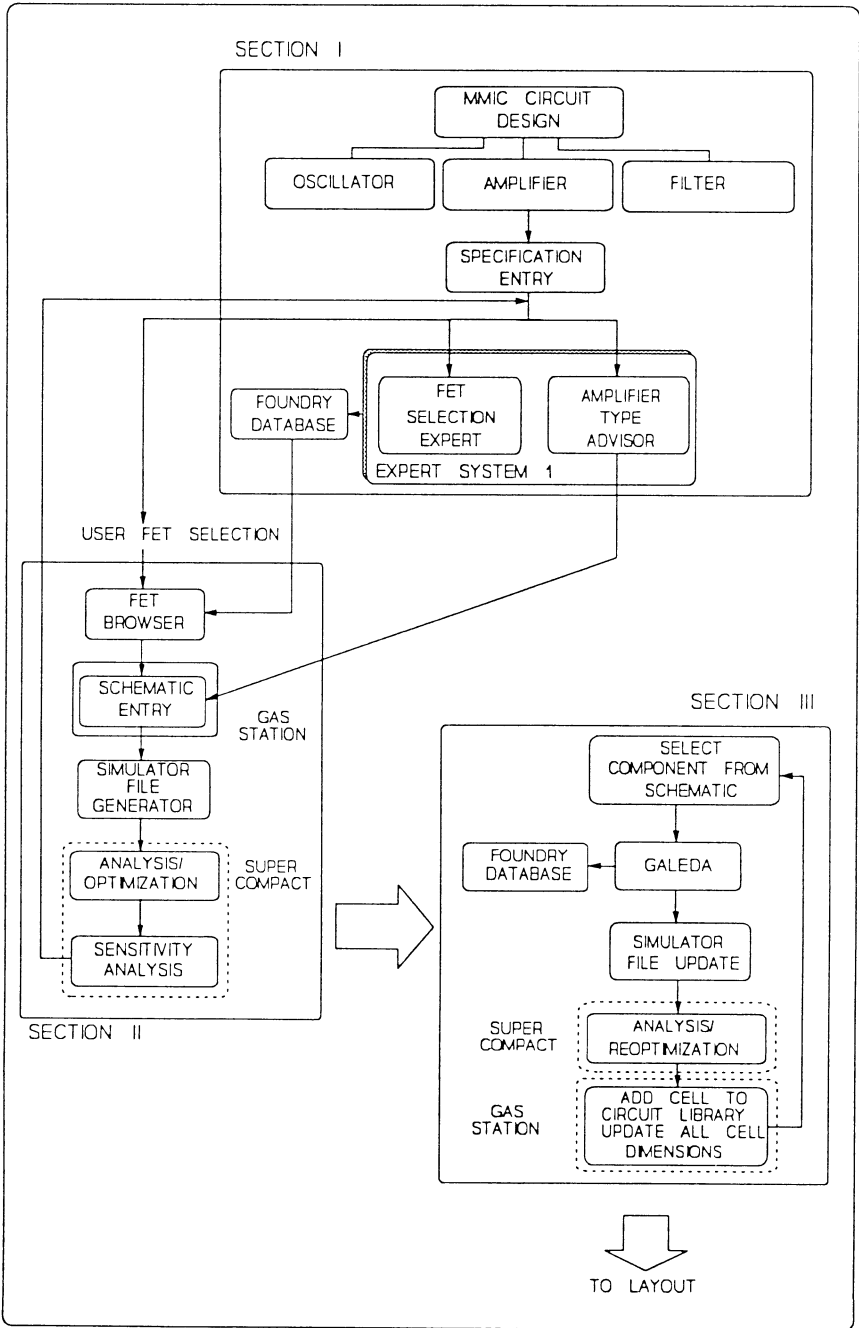


Figure 2 : MMIC Design Framework



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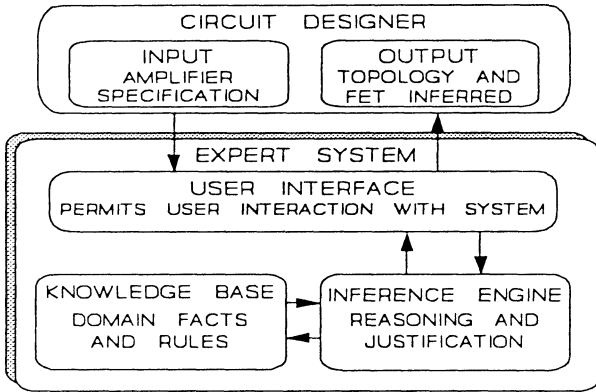


Figure 3 : Expert System Structure

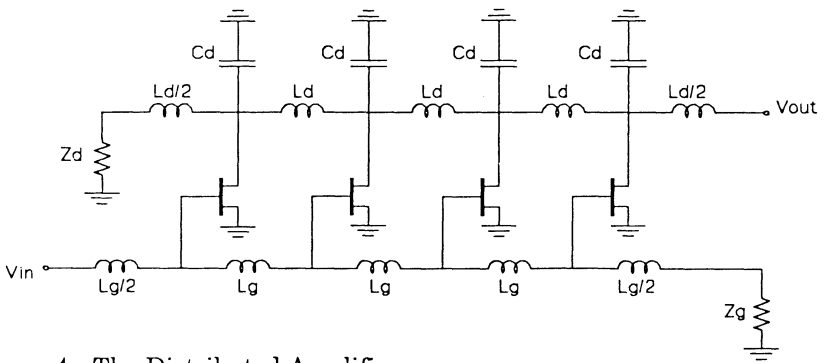


Figure 4 : The Distributed Amplifier

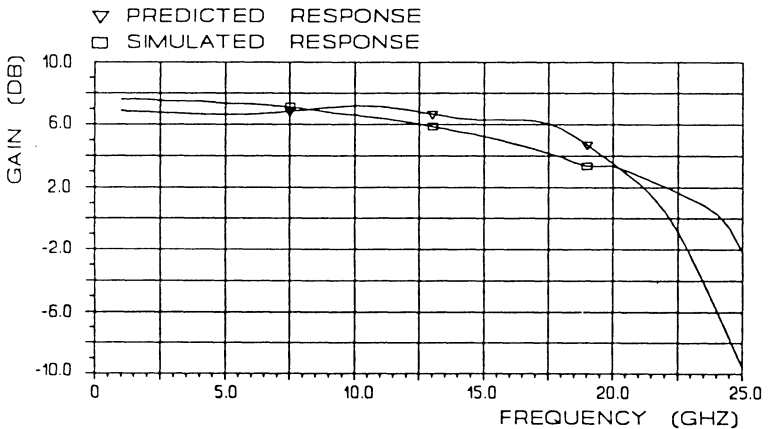


Figure 5 : Comparison of Predicted and Simulated Results