Nonlinear deformation and crack interactions in semiconductor packages

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Abstract

In this study, three-dimensional enriched crack tip elements were employed to analyze interfacial cracking problems encountered in electronic packaging. These elements are located at the crack tip region and contain the correct 3-D crack tip displacement and singular strain fields with unknown stress intensity factors. Using enriched elements, the elastic-plastic behavior of solder balls and interaction effects with nearby cracks in a flip-chip semiconductor package were investigated. Applying periodicity boundary conditions, a slice near the central region of the device was considered. Results from two differently shaped interfacial cracks near the fillet region are presented. Including plasticity effects on the solder balls, the interaction between plastic deformation and fracture parameters was investigated (elastic crack tip behavior). The two interfacial crack configurations are; a vertical crack between the fillet and the Si-chip, and an “L” shaped crack between the underfill material and the chip. The results from these calculations showed that plastic deformation, especially on the outermost solder ball, is affected by the presence of a crack in its vicinity and vice versa. It was observed that the plastic strains increase as the crack tip approaches the outermost solder ball. Depending on the type of crack under consideration, the fracture parameters can also vary significantly along the crack front even for the straight through cracks presented in this paper. In studying the “L” shaped crack, it was concluded that inclusion of crack surface contact is critical for accurate determination of plastic strains and fracture parameters.
1 Introduction

The trend in the development of new semiconductor packages is towards low cost, fine pitch, high performance and high reliability devices [1]. Also, the need for smaller packages is increasing in a variety of applications. This is due to restricted size specifications in many electronic devices. This trend, therefore, has made assurance and analysis of mechanical reliability of these devices critical.

Major mechanical failures of semiconductor packages are due to severe thermal loading conditions and moisture absorption from the environment. Since a semiconductor package is composed of different material layers, thermal stresses are generated when the device experiences temperature changes. This is mainly due to differences in the material properties of the constituent materials. Therefore, when thermal conditions are severe enough, mechanical failure of components in the package or interfacial cracking can be observed. These thermal conditions can be experienced by the package during the fabrication process and/or during the service life. Moisture induced stresses can also be harmful to semiconductor packages. Moisture, diffusing into the package from the environment, can accumulate in defects. With increasing temperature during the solder reflow process or during the service life of the package, the available moisture can become pressurized, forcing the existing defects to grow and resulting in the failure of the device.

In Fig. 1, a flip-chip semiconductor package is shown. The package consists of a silicon-die, a substrate, solder balls and underfill material. Solder balls and the underfill material are located between the silicon-chip and the substrate. Fig. 1(b) shows the top view of the device.

![Figure 1: A Flip-Chip Package, (a): General View, (b): Top View.](image)

In a semiconductor package such as the one shown in Fig. 1, the main material property mismatch is the coefficient of thermal expansion (CTE) difference between the silicon-die and the substrate/printed circuit board. This high CTE mismatch produces high shearing and peeling stresses in the outer regions (free-edge) of the package when a temperature change occurs. Among possible failure modes, interfacial debonding along the underfill-chip or underfill-substrate interfaces and
mechanical failure of solder joints are the most common. When the semiconductor package experiences temperature changes, the relative shearing displacements between the Si-chip and the substrate are accommodated by the solder balls. Thus, the solder balls close to the free-end region of the package are subjected to high shearing stresses. It is generally the case that, under severe thermal conditions, solder balls deform elasto-plastically. Underfill material, on the other hand, acts as a protective and supportive material within the package. Nevertheless, interfacial debonding between the underfill and the chip or the underfill and the substrate has also been observed in semiconductor packages.

When thermal conditions on the semiconductor package are severe enough, an interfacial crack may nucleate on the chip/fillet interface from a corner location and propagate vertically towards the lower corner of the chip. In addition, due to local stresses and a weak interface in this region, the crack turns and continues propagating underneath the chip in the horizontal direction [2]. It should be noted that if this happens, the outermost solder ball is most probably the first site for mechanical and electrical failure. Depending on the thermal loading conditions, geometry and boundary restraints, this crack may continue on the same interface separating the solder ball from the chip or run into the solder ball. Both of these cases are not desirable and can cause loss of electrical connections between the chip and the substrate/printed circuit board in these damaged locations.

In this study, a three-dimensional finite element model is used to analyze the characteristics of three-dimensional interfacial fracture problems encountered in semiconductor packaging applications. Also, by including the materially nonlinear behavior of solder balls, the interaction between plastic deformation of the solder balls and the fracture parameters of a neighboring interface crack is investigated [3,4]. To compute the fracture parameters, i.e., mixed-mode stress intensity factors and energy release rates, a specialized three-dimensional finite element program, FRAC3D, was developed [5]. FRAC3D uses the “enriched finite element” method for fracture analysis. Details of the 3-D enrichment methodology can be found in Ref.’s [3, 6-8].

2 Interface crack and solder ball interactions in flip chip packages

The package analyzed is a square Silicon die (0.686 mm thick, 20.32 mm wide), bonded to a square substrate (1.016 mm thick, 23.0125 mm wide). The bond thickness between the die and the substrate is 0.0762 mm, with the bond composed of solder balls (~25% by volume) and epoxy underfill. By taking advantage of periodic placements of solder balls under the die, a slice near the central region of the package is modeled (Fig. 2). In the model, a realistic underfill fillet at the edge of the die is also included (the fillet has a 45° inclination angle and intersects the vertical edge of the chip at half thickness of the chip). Since the package is not constrained during the fabrication process, the solder balls that are close to free-end are more
susceptible to mechanical damage. Therefore, to reduce the number of three-dimensional finite elements in the model, only the last four solder balls were modeled and the remaining constituents in the underfill layer were considered to be one material for which the properties were calculated based on the volumetric ratio of underfill and solder. To validate the 4-solder model, another model with 8 solder balls was also created and good agreement was obtained between the two models [3]. Material properties of the Si-chip and solder, [9], are given in Table 1 ($\theta$ is the absolute temperature). Material properties of FR-4 substrate and epoxy underfill material are given in Table 2. Poisson’s ratios for FR-4 and underfill material are 0.39 and 0.3, respectively. The coefficient of thermal expansion (CTE) of FR-4 is orthotropic and given by, $\alpha_x = 15 \times 10^{-6}$ $1/°C$, $\alpha_y = 57 \times 10^{-6}$ $1/°C$, $\alpha_z = 15 \times 10^{-6}$ $1/°C$.

### Table 1: Material Properties of Si-Chip and Solder [9].

<table>
<thead>
<tr>
<th>Property/Material</th>
<th>Si-Chip</th>
<th>Solder</th>
</tr>
</thead>
<tbody>
<tr>
<td>Elastic Modulus (GPa)</td>
<td>129.9</td>
<td>61.6-0.04508 $\theta$</td>
</tr>
<tr>
<td>Poisson’s Ratio</td>
<td>0.279</td>
<td>0.4</td>
</tr>
<tr>
<td>CTE ($10^6$ $1/°C$)</td>
<td>3.3</td>
<td>25.0</td>
</tr>
<tr>
<td>Yield Stress (MPa)</td>
<td>N/A</td>
<td>101.6-0.227 $\theta$</td>
</tr>
<tr>
<td>Tangent Modulus</td>
<td>N/A</td>
<td>0.05 $E(\theta)$</td>
</tr>
</tbody>
</table>

### Table 2: Material Properties of Substrate and Underfill.

<table>
<thead>
<tr>
<th>$E$ (MPa) $FR-4$</th>
<th>$E$ (MPa) Underfill</th>
<th>CTE ($10^6$ $1/°C$) $FR-4$</th>
<th>CTE ($10^6$ $1/°C$) Underfill</th>
</tr>
</thead>
<tbody>
<tr>
<td>18100 (7°C)</td>
<td>5029 (22°C)</td>
<td>28 (27°C)</td>
<td></td>
</tr>
<tr>
<td>17700 (27°C)</td>
<td>4325 (43°C)</td>
<td>29 (47°C)</td>
<td></td>
</tr>
<tr>
<td>17200 (47°C)</td>
<td>3921 (65°C)</td>
<td>31 (67°C)</td>
<td></td>
</tr>
<tr>
<td>16800 (67°C)</td>
<td>3642 (86°C)</td>
<td>35 (87°C)</td>
<td></td>
</tr>
<tr>
<td>16300 (87°C)</td>
<td>3311 (107°C)</td>
<td>39 (107°C)</td>
<td></td>
</tr>
<tr>
<td>15900 (107°C)</td>
<td>2859 (128°C)</td>
<td>48 (127°C)</td>
<td></td>
</tr>
<tr>
<td>15400 (127°C)</td>
<td>1960 (149°C)</td>
<td>49 (147°C)</td>
<td></td>
</tr>
<tr>
<td>15400 (147°C)</td>
<td>-</td>
<td>53 (157°C)</td>
<td></td>
</tr>
</tbody>
</table>

In this study, different interfacial cracks are studied and the effect of presence of an interface crack near the outermost solder joint is investigated. This effect includes changes in the elasto-plastic behavior of solder balls due to the existence of a neighboring crack and changes in the fracture parameters (mixed-mode stress intensity factors, strain energy release rate and mode mixity) due to plastic deformation of solder balls. Results from two different cracking configurations on the flip-chip package are presented. These crack types include 1) a vertical edge crack between the epoxy and Si-chip (Fig. 2) and 2) an “L” shaped crack between the epoxy and Si-chip (Fig. 3). For both crack types, the package is cooled down uniformly from 150°C to 25°C and there are no boundary restraints on the package other than the periodicity condition. To determine the fracture parameters, special temperature dependent enriched crack-tip finite elements are employed.
Although the underfill material enhances the solder joint life, it may be subjected to possible cracking along the chip-underfill or substrate-underfill interfaces during the manufacturing stages or the service life of the package. Experimental analyses of flip-chip assemblies have shown that cracks often initiate at the encapsulant (underfill)-chip interface due to the severe CTE mismatch between the two materials. This is due to the fact that a severe CTE mismatch will result in a strong interfacial shear stress concentration near the free edge and when the stress exceeds the bonding strength between the encapsulant and the silicon substrate, an interfacial crack will initiate from the edge, [10] (Fig. 2). When the thermal conditions are severe enough, this crack may propagate to the bottom corner of the chip and continue horizontally along the chip-underfill interface towards the outermost solder ball forming an L shaped crack, Fig. 3.

### 2.1 Vertical edge crack between chip and underfill material

This type of cracking (Fig. 2) is frequently observed in practical applications. In Ref. [10], the total strain energy release rate was evaluated by using the finite element method under constant-material property and elastic conditions for a similar type of interfacial crack. Here, the problem is solved considering temperature dependence of the constituent materials (including temperature dependent enriched crack tip finite elements) and plasticity effects on the solder balls. Finite element calculations have been performed for eight different crack lengths, from \( a = 0.038 \) mm to \( a = 0.318 \) mm. The crack length, \( a \), is measured from the upper corner of the fillet where it touches the vertical edge of the chip.

In Fig. 4 and Fig. 5, the strain energy release rate and phase angle, \( \psi = \arctan(k_y/k_x) \), are plotted, respectively, as a function of crack length for the symmetry point on the crack front. Note that the strain energy release rate initially increases and then starts decreasing as it approaches the internal 90° edge. When the crack length becomes \( a = 0.318 \) mm, examination of deformed configuration reveals that the crack surfaces come into large-scale contact [3]. This is reflected by a slight increase in the strain energy release rate and a sudden drop in the phase angle.
Therefore, this crack length case needs to be restudied by including the appropriate contact algorithm in the analysis. Analysis of effective plastic strain distributions on the solder balls reveals that the effect of the vertical cracking on the plastic deformation of the solder balls is negligible, i.e., there are no significant differences in the effective plastic strain distributions on the solder balls for different crack lengths. This is mainly due to two factors: 1) one of the materials involved in the interfacial cracking is very stiff (silicon-chip) compared to the other material (underfill) and 2) for the longest crack length studied, the crack tip is more than half a solder ball away from the outermost solder interconnection. Therefore, the vertical crack on the fillet/chip interface does not have a significant effect on plastic deformation in the solder balls and vice versa [3].

2.2 L shaped interface crack between chip and underfill material

In practical applications, it has been observed that the vertical edge crack studied in the previous section can propagate to the lower corner of the silicon-die. Due to the high shearing stresses in this region, it can, then, turn towards the outermost solder ball and start propagating horizontally along chip-underfill interface [2]. An interesting feature of this type of “L” crack is that for negative $\Delta T$, the lower corner region of the silicon-die and the corresponding corner region on the fillet come into contact. The effect of contact on fracture parameters and plastic deformation of solder interconnections is addressed in this section.

Three different crack lengths were studied, and results from the smallest and largest crack lengths are given in this section. These include strain energy release rates and phase angles along the crack front. Effective plastic strains are also plotted along the chip-underfill/solder interface. The crack length, $a$, is measured from the lower corner of the Si-die. For each crack length, two different finite element

Figure 4: Strain Energy Release Rate vs. Crack Length, A-A', $\Delta T = -125 \, ^\circ C$.

Figure 5: Phase Angle vs. Crack Length, A-A', $\Delta T = -125 \, ^\circ C$. 
calculations are performed. In the first case, the penetration at the corner between the die and the underfill is prevented. In the second case, the penetration is allowed. The contact condition is simulated by tying the contacting nodes, which are located along the lower edge of the chip and the corresponding corner edge of the fillet, in the horizontal (x) direction to simulate frictionless contact. In the case where the two edges are allowed to pass through one another, which is not possible in reality, the tied node constraint is removed. As would be expected, the results from the analysis in which the two edges are tied together in the horizontal direction result in significantly different stress intensity factors.

In Fig. 6 and Fig. 7, the total strain energy release rate and the phase angle are plotted with respect to temperature change at three locations on the crack front ($a = 0.0127$ mm). In this case, the penetration between the chip and the fillet is prevented. Note that, there is some variation in the fracture parameters along the crack front. Fig. 8 shows the behavior of strain energy release rate for the same locations on the crack front with the condition that the prescribed edges are allowed to pass through one another. Note the very large increase in the strain energy release rate compared to Fig. 6. This increase is due to the fact that the edge of the fillet is allowed to pass through the vertical edge of the chip resulting in greater relative shearing and crack opening displacements in the vicinity of the crack tip.

Additional fracture results for $a = 0.0508$ mm are presented in Fig. 9 and Fig. 10 for the case where penetration of the contact surfaces are prevented (contacting condition). Note that, at the end of the thermal loading, the variation in the strain energy release rate along the crack front becomes quite large (Fig. 9). Examination of Fig. 9 shows that the energy release rate on the solder mid-plane ($C-C'$) is almost twice as large as the energy release rate on the plane between solder balls. Such an energy release rate variation along the crack front should result in a higher crack.
growth rate on the solder mid-plane. This difference is mainly attributed to the plastic deformation of the solder interconnections and to the differences in temperature dependent properties of the solder and underfill material. It should also be noted that the strain energy release rate increases with increasing crack length.

Figures 8 and 9 depict the strain energy release rate vs. temperature change, $a = 0.0127$ mm, Penetration Allowed. Figures 10 and 11 show the phase angle vs. temperature change, $a = 0.0508$ mm, Penetration Prevented. Figures 11 and 12 depict the effective plastic strain distributions in the solder balls, on the solder-mid plane (C-C'), at the chip-underfill interface, for different crack lengths. These results are given for both contacting and non-contacting conditions. Note the large increase in plastic deformation on the outermost solder ball as the crack length increases. As expected, the non-contacting condition estimates a higher permanent deformation on the outermost solder ball. This is again due to the fact that, the relative shearing displacement at the end of the package is
suppressed in the contact case by preventing the fillet corner from passing through the lower corner of the chip. Therefore, a lower estimate of plastic damage on the outermost solder ball is obtained using the contact condition.

![Effective Plastic Strain Distribution for Different Crack Lengths, Penetration Allowed.](image1)

**Figure 12:** Effective Plastic Strain Distribution for Different Crack Lengths, Penetration Allowed.

![Close-up View of Effective Stresses in The Fillet Region, No Penetration.](image2)

**Figure 13:** Close-up View of Effective Stresses in The Fillet Region, No Penetration.

Although prevention of the two edges from passing through one another reduces the strain energy release rate and permanent damage on the outermost solder ball, it causes much higher stresses near the contacting corner of the fillet. This can be seen in Fig. 13, where, the effective stress distribution is shown for the case $a = 0.0381$ mm. Thus, this internal corner is a likely site for the formation of a new crack that will propagate outwards from the corner into the fillet.

### 3 Conclusion

Three-dimensional enriched finite elements were used to solve interface crack problems encountered in semiconductor packaging applications. For this purpose, a three-dimensional finite element program, FRAC3D, was developed. Temperature-dependent elasto-plastic behavior was also incorporated in the program to realistically simulate deformations in solder connections.

The main purpose of this study was to investigate the mutual interaction effects between the plastic deformation of solder balls and fracture parameters for a nearby interfacial crack. The results show that when a crack approaches the outermost solder ball in a flip-chip package, there will be an increase in both the solder ball plastic deformation and the crack tip strain energy release rate. In addition, the presence of a solder ball in the path of an advancing crack front, causes a variation in the strain energy release rate, resulting in non-uniform growth rates along the crack front. Finally, it was shown that consideration of crack surface
contact is essential for accurate determination of fracture parameters under these complex loading conditions.

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References


