NON-DESTRUCTIVE EDDY CURRENT MEASUREMENTS FOR SILICON CARBIDE HETEROSTRUCTURE ANALYSIS

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ABSTRACT

Heterostructures consisting of two different silicon carbide (SiC) polytypes have been of interest for several years, promising application in the field of UV LEDs and sensors. Direct bonding (also called diffusion welding) is a technology that could possibly be used for manufacturing SiC heterostructures. The technology has been proven in experimental production of power devices for ohmic- and Schottky-contacts to SiC, as well as high-voltage stacks. The fabrication of heterostructures has not been successful yet, due to the hardness of SiC as well as the high temperature and pressure needed for accomplishing a reliable joint between two SiC polytype wafers. No thorough analysis is available in studying the quality of achieved contacts and the causes for their short breakdown in time. The intention is to try higher temperatures than used before for direct bonding of SiC different polytypes. To understand the contact failure causes there is a need for quick non-destructive measurements of the heterojunction properties in the depth of bonded layers. Eddy currents measurements seems to be the best solution for further investigation. Simulations with COMSOL Multiphysics general-purpose simulator are carried out with different electrode shapes and different electrode placements. The numerical simulation and test equipment building results at the Thomas Johann Seebeck Department of Electronics are analyzed and discussed.

Keywords: SiC heterostructure, direct bonding, eddy currents, non-destructive measurements.

1 INTRODUCTION

Silicon carbide (SiC) is the only compound material of silicon and carbide materials existing in the solid phase under normal conditions. It has numerous applications in different fields of technology, such as aircrafts, automobiles, spacecrafts, power supplies, communications to name a few. In aircraft industry, SiC is applied to keep some devices, mounted in aero-surface areas of the aircraft, functioning reliably under high- temperature conditions. In public electric power distribution systems, SiC is applied in electronic power supplies in extreme situations where producing excess power reserve is very important. In automobile and transportation industry SiC is used to design circuits for automobile to work in temperatures above 125°C, to insure the optimal functioning of the automobile engine [1].

SiC heterostructures are relatively new type of semiconductor heterostructures that consist of one material in different hetero-polytypical structures which differ from each other only by crystal structures. High-performing heterostructures need to be relatively defect-free and well lattice-matched. In technology, cubic and hexagonal SiC polytypes are widely used, such as 3C-SiC (also called β-SiC polytype), 4H-SiC and 6H-SiC (also called α-SiC polytype) (see Fig. 1) [2].

SiC heterostructures formed by epitaxial growth of 3C-SiC polytype layer on top of 6H-SiC bulk material has its application in production of electronic devices. For microelectromechanical systems (MEMS), 3C-SiC polytype is more applicable, while 4H or 6H-SiC polytypes are more used in blue light-emitting diode and UV photodetectors [4]. Crystal structures of the three SiC polytypes and their respective atomic arrangements are illustrated in Fig. 2.

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(from left to right 3C-SiC, 4H-SiC and 6H-SiC) [3].

Figure 1: Optical images of three most common SiC polytypes.

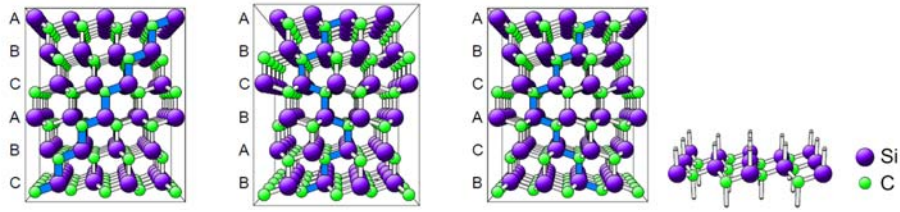

Figure 2: Crystal structures of three most common SiC polytypes and the arrangements Si and C atoms in them [5].

As it can be seen from Fig. 2, SiC consists of equal number of silicon and carbide atoms and each atom inside the crystal structure is bonded to four atoms of other material in a tetrahedral bonding configuration. Only three types of atomic arrangement can be found: A, B and C. Each SiC polytype is consisted of the same layers but in different A, B and C arrangements [6].

2 DIRECT BONDING TECHNOLOGY FOR FABRICATION OF SIC HETEROSTRUCTURES

Direct bonding (DB) technology, also known as diffusion welding, allows fabrication of new combination of materials which haven't ever existed in the world before since it couldn't be realized by traditional epitaxial growth techniques. It suggests the process of bringing into direct contact two flat and mirror polished wafers of different materials regardless of their crystal structure (amorphous, polycrystalline, or single crystal). Usually this process takes place in room temperature. The surfaces of the wafers adhere each other by Van der Waals forces present among local dipoles on the attaching surfaces of opposite materials. In this case, the experiments have shown that the bonding of the wafers is not firm comparing with covalent or ionic bonding. Therefore, depending on specific applications, the wafers are thinned into micrometer or even nanometer sizes and are bonded together through heating them, which make the bonds stronger. When the wafers of dissimilar materials are subject to DB, the strengthening of the bonding through heating treatment depends on the difference in thermal expansion coefficients of those materials and whether the mechanical stress is exposed for strengthening the bonding without causing de-bonding, wafer sliding or fracture [7].

Specific electrical or physical properties can be achieved for new heterostructures formed by direct bonding of different polytypes of SiC material, which are not possible to achieve

through traditional epitaxial growth methods. For strengthening the bonding, the polytypes are exposed to high temperature and the pressure is applied to them.

Mechanical defects emerged during DB technology are due to types of materials, materials' surface preparation or materials' damages related to inappropriate handling. They can be in the form of cracks, fractures resulted from wafer surface polishing (Fig. 3), sawing the wafers (Fig. 4), unbonded areas, voids and so on [8].

It is discussed the surface activated SiC-SiC wafer bonding [11]. Owing to this method the DB of SiC-SiC wafers can be achieved at the room temperature in comparison with past DB methods operated in high temperatures and thermal stressed exposed to the wafers. It can be seen from Fig. 5 that SiC wafers are bonded together very strongly and, therefore, the cracks and fractures can be seen in the interface between adhesive layer and the wafer.

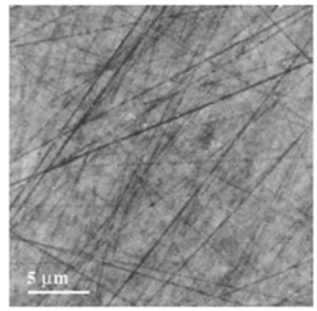

Figure 3: SiC wafer surface polishing scratches [9].

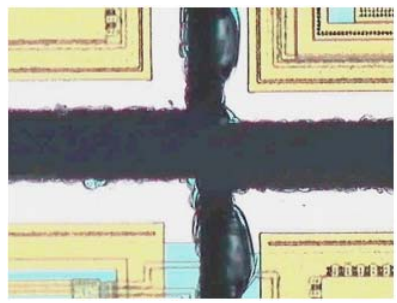

Figure 4: Corner cracks caused by wafer sawing [10].

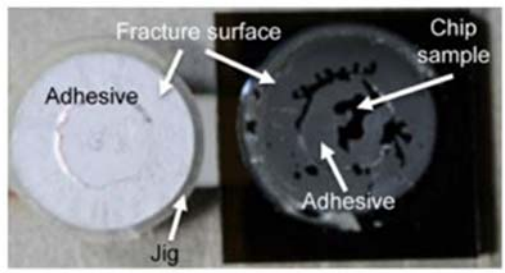

Figure 5: Fractures at the interface between the adhesive layer and the sample [11].

The defects can also be formed when two SiC polytype wafers are firstly exposed to hydrophilic surface treatment and then are directly bonded together. In this case the defects are in the form of thin water layer remaining in the interface between two layers, which itself resulted in formation of SiO_x insulation layer. Therefore, in some places of the bonding interface two wafers are directly attached together, in other places they are separated by SiO_x insulation layer (see Fig. 5).

3 NON-DESTRUCTIVE EDDY CURRENT MEASUREMENT METHODS FOR WAFER DEFECT INSPECTION

Non-destructive measurement methods have been widely used recent years since their system structure is simple and reliable. In addition to that, they can be applied for testing wide range of different materials of semiconductor wafers even in extreme conditions with high temperature and pressure. These methods allow us to measure defects of the wafers under test without the probe having direct contact with the wafer. These defects can result in the degradation and low performance of the semiconductor material [13].

Among those methods, eddy-current (EC) measurement method is the most efficiently used for wafer surface defect characterization. The principle of this method is based on the electromagnetic model and reflectometry [14]. Fig. 7 illustrates the basic principle of EC measurement method.

In Fig. 7 the coil probe is connected to the alternating current (AC) circuit and is generating alternative magnetic field and magnetic flux interacts and penetrates the wafer located below. As a result, the circular eddy currents are created on the surface and inside the wafer which are flowing perpendicular to the magnetic field flux lines, based on Faraday's Law. These eddy currents themselves create secondary magnetic field which flaws opposite direction to the primary magnetic field, according to Lenz's Law. By measuring the changes

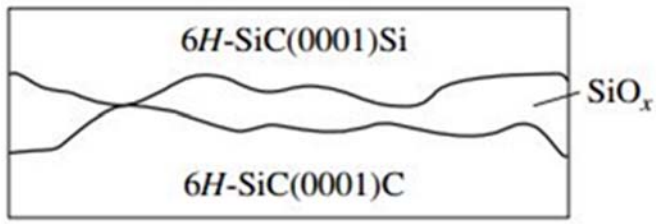

Figure 6: SiC-SiC wafer bonding with SiO_x insulator layer as a defect [12].

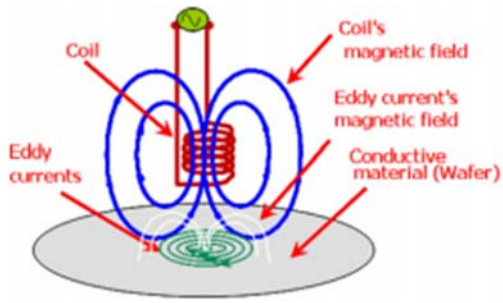

Figure 7: Principle of EC measurement method [15].

in the resistance and inductive reactance as a complex impedance of the coil, so as the coil voltage, the information can be gathered about the defects of the wafer material under the test [16].

Different researches have been done for the implementation of eddy current measurement method for inspection of defects on the surface of the wafer. Magneto-optic imaging method has been proposed for detecting the defects on the surface of semiconductor wafer [17]. In this method, eddy current is being induced into the wafer and the magnetic flux generated by eddy currents is being located by implementing the Faraday rotation effect. As a result, magneto-optic image is created which, being processed for the removal of the unwanted noise, is giving the clear picture for the cracks or curvatures on the surface of the wafer. Subminiature eddy current transducer is suggested for studying semiconductor material [18].

Based on the suggested structure of the system and technical data provided in the method, only small areas of the tested wafer can be studied and analyzed since magnetic field has much constraints. The finite element method is used for eddy current testing to detect flaws on the surface of the conducting material [19]. This method is implemented using COMSOL-Multiphysics simulation software. Finally, the mathematical model is used to describe eddy current technique for detection and examination of the defects embedded in aeronautical in-service pieces [20]. After that, the finite element method is used to make mathematical model of the eddy current technique through predicting the interaction of eddy current with wafer defects.

5 METHODOLOGY

In this paper, the novel method for eddy current measurements has been suggested for inspection the defects in the depth of semiconductor wafer in the bonded layer of two SiC polytypes. Finite element method has been applied to investigate the interaction of induced eddy currents and the defects on the interface of direct bonding of two materials. COMSOL Multiphysics general-purpose software has been used for creating the model and for simulations.

In Fig. 8 β-SiC and α-SiC polytype layers have been directly bonded together with the thickness of 300μm each. As a defect emerging in the direct bonding contact, 20μm SiO_2 insulation layer is used. Coil probe is made of copper material, coil wire cross-section area: 1e-2 mm^2, coil diameter: 5 mm^2 and number of turns: 1200. As the electric parameters for the coil probe, coil inductance has been chosen: 15.309e-3 H, relative permeability: 1, relative permittivity: 1 and electric conductivity: 5.9e+7 S/m. As the input signal for the probe-wafer system, alternative current has been given with the magnitude of 0.025 A. The coil probe for eddy current measurements is connected to alternating current source and is shifted with 45° angle with respect to the wafer surface. Therefore, magnetic flux is penetrating on the 45° angle inside the wafer and the eddy currents, created perpendicular to flux lines, are cutting the insulation layer plane. This results in having more accurate information about the wafer material defect by measuring the change in the voltage and impedance of the coil probe. The measurements have been done using the wafer parameters given in Table 1.

6 EXPERIMENTAL RESULTS

The simulations have been conducted by COMSOL-Multiphysics general purpose software using finite model of the system. The coil probe and wafer have been placed in the air medium. The measurements have been conducted at high frequencies of the input signal, specifically at 3MHz and 5MHz. The simulations have been done with vertical coil placement and for 45° rotated coil placement relative to the wafer surface. Three wafer configurations

have been simulated, without any defect, with defect covering the full simulated area and with half area defect. The magnetic field distribution, magnetic flux density and eddy current density have been shown for each case in Figs 9–20. Fig. 21 illustrates the wafer cut with defect, where we can notice that eddy currents do not penetrate the defect layer (insulation layer).

a)

b)

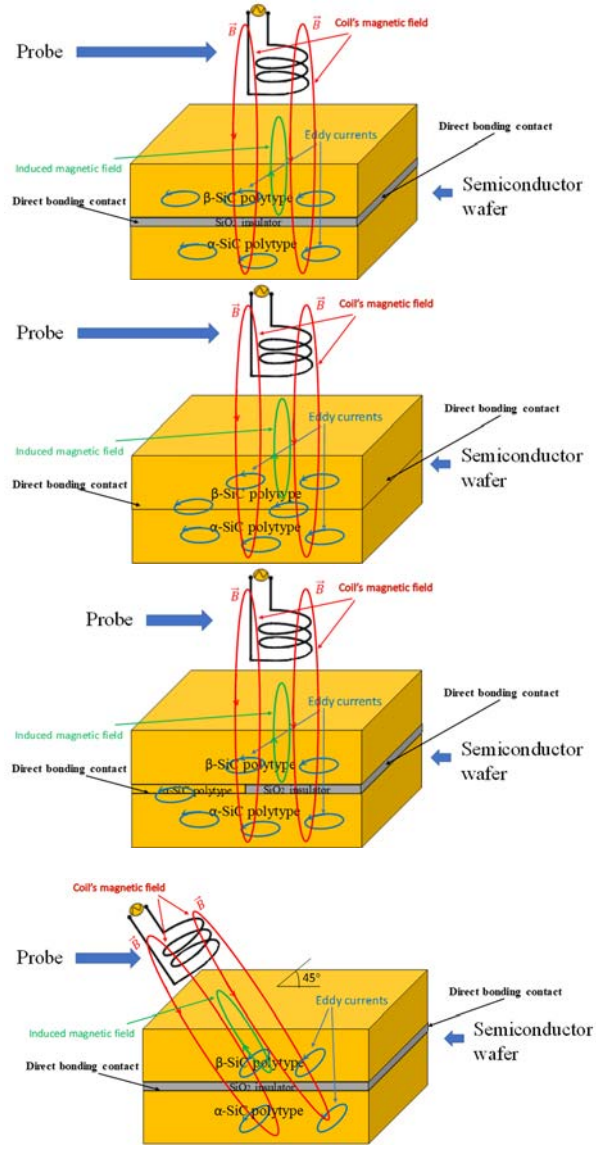

Figure 8: The model of the proposed method. (a) The coil probe is placed vertically relative to the wafer (with full defect edge, no edge and half defect edge); b) The coil probe is placed under 45° angle relative to the wafer (with full defect edge, no edge and half defect edge).

b)

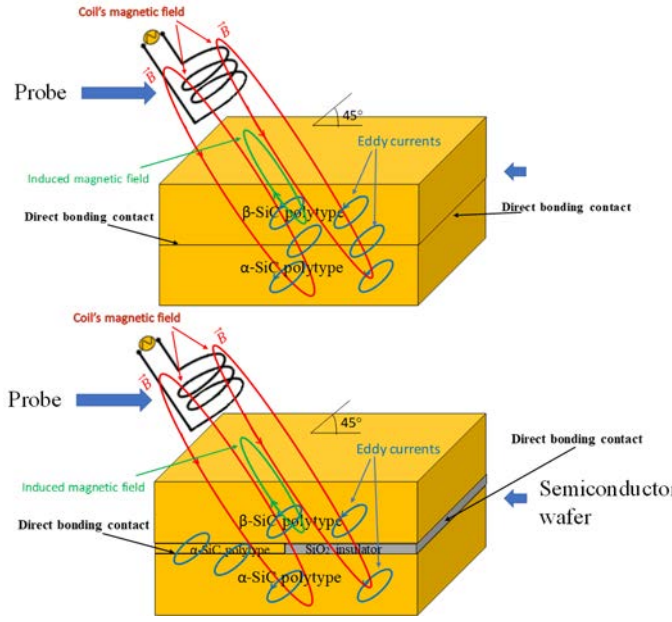

Figure 8 (Continued.)

Table 1: Wafer parameters.

Type of material	β-SiC polytype	SiO_2 insulator	α-SiC polytype
Layer thickness, [mm]	0.3	0.02	0.3
Relative permeability	1	1	1
Relative permittivity	9.7	9.7	3.9
Electric conductivity, [S/m]	1e-6	1e-16	

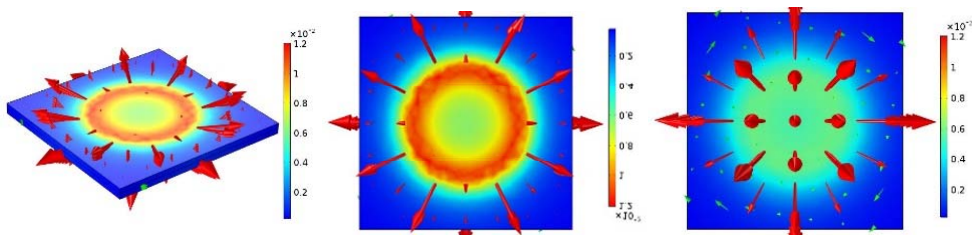

Figure 9: Coil probe is placed vertically relative to the wafer with no edge. The simulation is conducted at 3MHz.

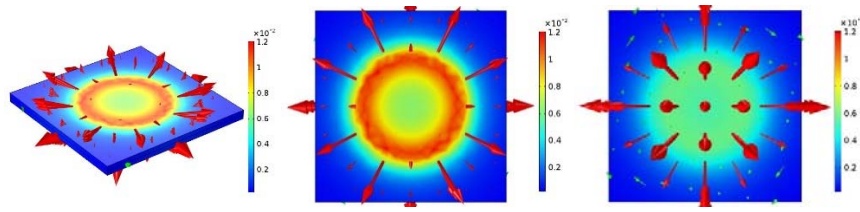

Figure 10: Coil probe is placed vertically relative to the wafer with no edge. The simulation is conducted at 5MHz.

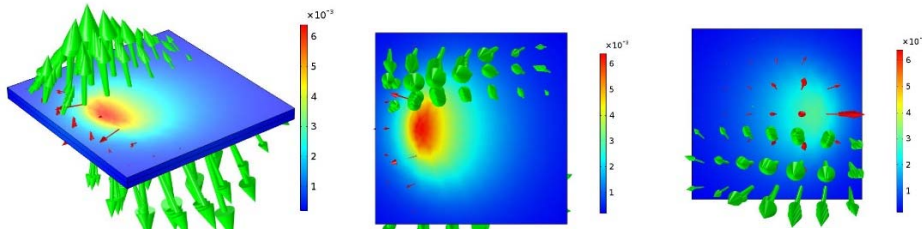

Figure 11: Coil probe is placed under 45° angle relative to the wafer with no edge. The simulation is conducted at 3MHz.

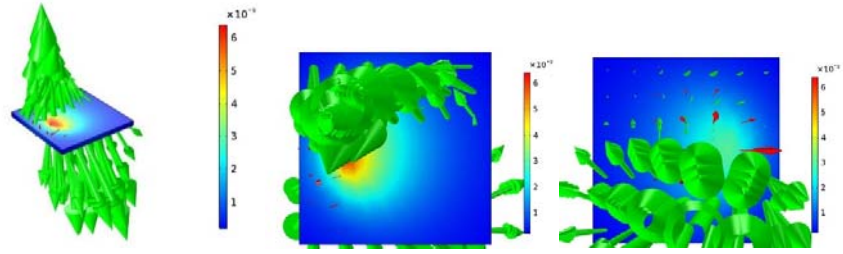

Figure 12: Coil probe is placed under 45° angle relative to the wafer with no edge. The simulation is conducted at 5MHz.

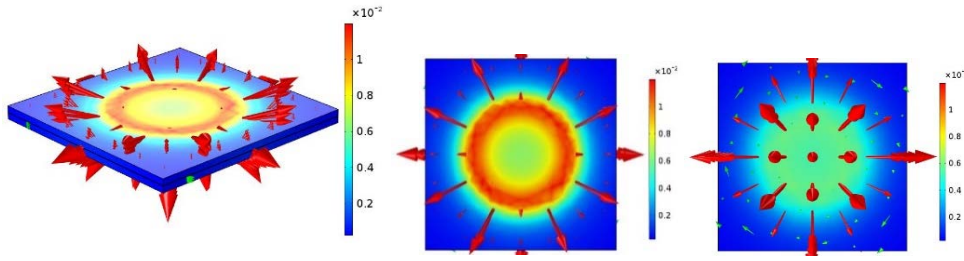

Figure 13: Coil probe is placed vertically relative to the wafer with full defect edge. The simulation is conducted at 3MHz.

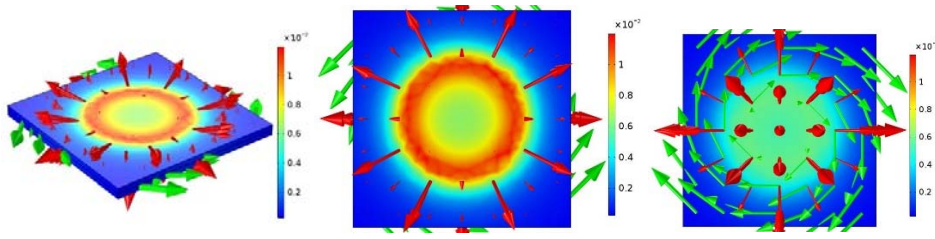

Figure 14: Coil probe is placed vertically relative to the wafer with full defect edge. The simulation is conducted at 5MHz.

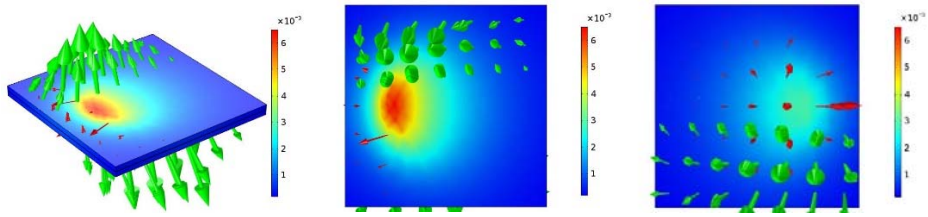

Figure 15: Coil probe is placed under 45° angle relative to the wafer with full defect edge. The simulation is conducted at 3MHz.

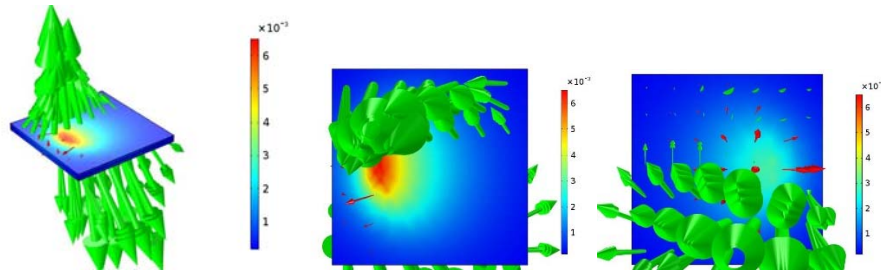

Figure 16: Coil probe is placed under 45° angle relative to the wafer with full defect edge. The simulation is conducted at 5MHz.

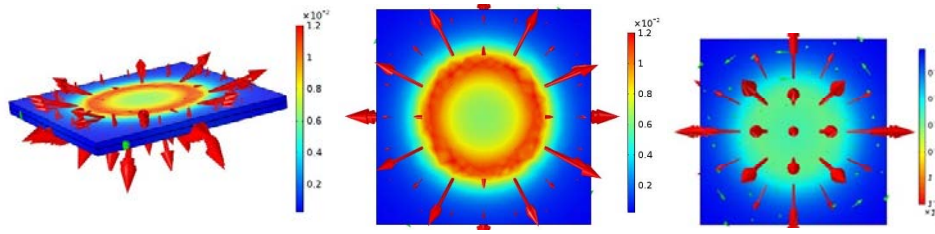

Figure 17: Coil probe is placed vertically relative to the wafer with half defect edge. The simulation is conducted at 3MHz.

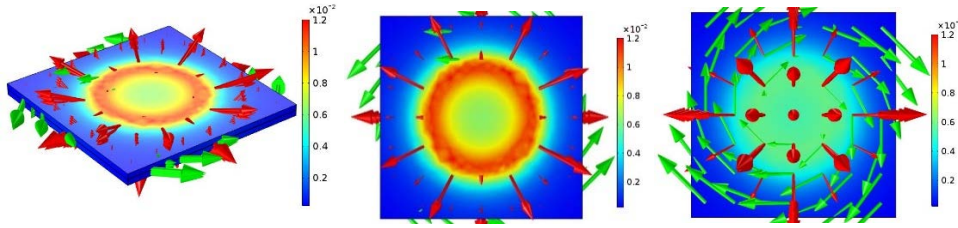

Figure 18: Coil probe is placed vertically relative to the wafer with half defect edge. The simulation is conducted at 5MHz.

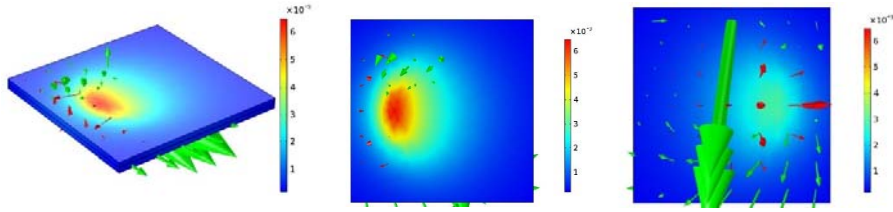

Figure 19: Coil probe is placed under 45° angle relative to the wafer with half defect edge. The simulation is conducted at 3MHz.

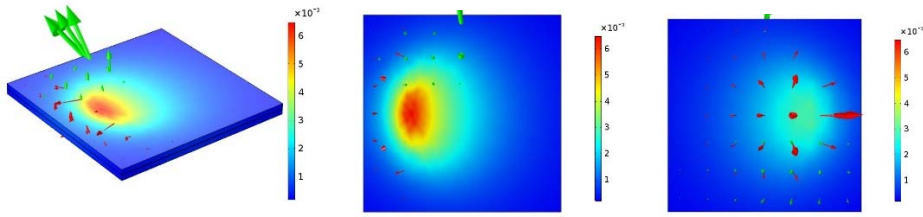

Figure 20: Coil probe is placed under 45° angle relative to the wafer with half defect edge. The simulation is conducted at 5MHz.

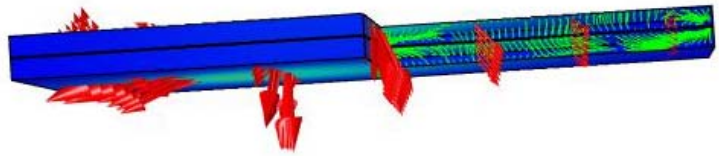

Figure 21: The cut of the wafer showing that eddy currents exist only in SiC polytypes.

Table 2: Coil impedance (Z_{ip}) simulation results for the coil probe placed vertical relative to the wafer at different frequencies.

	No defect	Full defect	Half defect
Z_{ip} at 3 MHz, [Ω]	99.307+288.754e3i	99.091+288.577e3i	99.111+288.576e3i
Z_i at 5 MHz, [Ω]	273.045+481.252e3i	272.444+480.957e3i	272.499+480.955e3i

Table 3: Coil impedance (Zi) simulation results for the coil probe placed under 45° angle relative to the wafer at different frequencies.

	No defect	Full defect	Half defect
Z_i at 3 MHz, [Ω]	103.024+288.697e3i	102.964+288.684e3i	102.963+288.812e3i
Z_i at 5 MHz, [Ω]	283.377+481.158e3i	283.209+481.135e3i	283.207+481.349e3i

The measurement results for the coil parameters, specifically for coil voltage impedance and inductance have been shown in Tables 3–4.

7 CONCLUSION

The simulations show the possibility to investigate mechanical defects buried deep in semiconductor material with the method of eddy currents. The difference in impedance real part varies in the range up to 3% in real part (Tables 2, 3). The defect edges can be detected with coil placed under angle (comparing Figs 11 and 15 with no edge and Fig. 19 with defect edge). The frequency of the simulations was based on planned following experiments, similar to the ones used for metal defects detection. The simulations show that there is no significant difference of potentially measurable parameters (coil impedance) in the applied frequencies range due to defects and the lower frequencies should be investigated. Still the resolution of the simulated system seems to be low for practical use, so alternative ideas like using two or more coils for current generation and measurements or combining with optical measurements should be considered.

As a future work, the dimensions of the coil can be investigated. Also for optimization of the probe-wafer system the range of the input current can be determined and methods for the signal processing can be discovered.

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REFERENCES

[1] Masri, P., Silicon carbide and silicon carbide-based structures, The physics of epitaxy. *Surface Science Reports*, 2002.
[2] Fissel, A., Artificially layered hetero-polytypic structures based on SiC polytypes: molecular beam epitaxy, characterization and properties. *Physics Reports*, 2002.
[3] Eriksson, J., *Transport properties at 3C/SiC interfaces. PhD thesis in Nanoscience,* Scuola Superiore of the University of Catania, 2010.
[4] Neudeck, P.G., Silicon Carbide Technology. *The VLSI handbook*, NASA Glenn Research Center, 2006.
[5] Starke, U., Bernhardt, J., Schardt, J. & Heinz, K., SiC surface reconstruction: relevancy of atomic structure for growth technology. *Surf. Rev. Lett. Preprint*, 1999.
[6] Fan, J. & Chu, P.K., Silicon carbide nanostructures. *Engineering and Material Processes*, Springer International Publishing – Switzerland, 2014.
[7] Gösele, U. & Tong, Q.Y., Semiconductor wafer bonding. *Annual Rev. Mater. Sci*., 1998.

[8] Shenkin, M., Korolkov, O., Rang, T. & Rang, G., Polytypic heterojunctions for wide bandgap semiconductor materials. *Materials Characterization VII*, WIT, Transactions on Engineering Sciences, 2015.
[9] Yushin, G.N., Kvit, A.V. & Sitar, Z., Transmission electron microscopy studies of the bonded SiC-SiC interface. *Journal of Materials Science*, 2005.
[10] Jacob, P. & Rothkirch, W., Unusual defects, generated by wafer sawing: Diagnosis, mechanisms and how to distinguish from related failures. *Microelectronics Reliability*, 2008.
[11] Suga, T., Mu, F., Fujino, M., Takahashi, Y., Nakazawa, H. & Iguchi, K., Silicon carbide wafer bonding by modified surface activated bonding method. *Japanese Journal of Applied Physics*, 2015.
[12] Ivanov, P.A. et al., Current – voltage characteristic of isotope SiC-SiC junctions fabricated by direct wafer bonding. *Semiconductors 2007*, pp. 921–924, 2007.
[13] Krupka, J., Contactless methods of conductivity and sheet resistance measurement for semiconductors, conductors and superconductors. *Meas. Sci. Technol.*, 2013.
[14] Loete, F., Le Bihan, Y. & Mencaraglia, D., Novel wideband eddy current device for the conductivity measurement of semiconductors. *IEEE Sensors Journal*, 2016.
[15] Krupka, J., Nguyen, D. & Mazierska, J., Microwave and RF methods of contactless mapping of the sheet resistance and the complex permittivity of conductive materials and semiconductors. *Meas. Sci. Technol. 22*, 2011.
[16] Abidin, I.M.Z., *Modelling and experimental investigation of eddy current distribution for angular defect characterisation*. School of Electrical, Electronic and Computer Engineering, Newcastle University, UK, 2010.
[17] Pan, Z., Chen, L., Li, W., Zhang, G. & Wu, P., A novel defect inspection method for semiconductor wafer based on magneto-optic imaging. *Journal of Low Temp. Phys.*, 2013.
[18] Dmitriev, S.F., Malikov, V.N., Sagalakov, A.M., Shevtsova, L.I. & Katasonov, A.O., Subminiature eddy current transducers for studying semiconductor material. *Journal of Physics: Conference Series 643*, 2015.
[19] Santandrea, L. & Le Bihan, Y., Using COMSOL-Multiphysics in an eddy current non-destructive testing context. *Proceedings of the COMSOL Conference*, 2010.
[20] Bennoud, S. & Zergoug, M., Modeling and simulation for 3D eddy current testing in conducting materials. *International Journal of Mechanical, Aerospace, Industrial, Mechatronic and Manufacturing Engineering*, **8**, 2014.