

## Analysis of deep level spectrum in GaAs $p^+-p-i-n-n^+$ structures

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### Abstract

This paper is devoted to the analysis of Deep Level Transient Spectroscopy (DLTS) of the background deep levels in GaAs  $p^+-p-i-n-n^+$  structures. It is known that A and B centers are observed in epitaxial layers of GaAs, grown by LPE in a hydrogen atmosphere. These two deep acceptor levels determine the minority carrier lifetime and the reverse recovery time ( $t_{rr}$ ) of rectifying devices respectively. The necessary switching time of GaAs rectifying devices is achieved by regulating the concentrations and the profile of A and B traps in  $pin$  layer. For undoped GaAs  $pin$ -structures with a thick  $i$ -layer, there is a problem in determining the direction of motion of the space charge boundaries upon application of reverse voltage to the diode structure. The boundary of the space charge region can propagate through  $i$ -layer and be displaced in  $p$ - and  $n$ -layer.

To ensure the reliability of statistical significance were treated great number (appr.100 pc.) chips, provided for the experiment. Chips were divided into groups according to their technological features of production. The presented spectra exhibit evidence of the presence of deep levels of the hole and electron type in all samples. But within each group, the configuration of the spectra is similar. And for each configuration correspond a certain set of output parameter characteristic. This will provide an opportunity for express DLTS control of the finished product and can be realized in on-line monitoring of the LPE process in order to optimize the dynamic characteristics of the devices.

*Keywords:* deep level traps, parameter extraction, DLTS, wide bandgap materials.



## 1 Introduction

It is well known that *pin*-diodes occupy a confident and ever-increasing position in RF and microwave devices. Reverse recovery time, and, therefore, the lifetime of minority carriers in such devices are a key factor in determining the frequency characteristics of the device. The lifetime in turn, depends on the processes of emission and capture of carriers at deep levels in the bandgap of the semiconductor.

The technological operations for making of GaAs rectifiers with various constructions are ordinary for semiconductor industry and not demand the high expenses. Epitaxial grown *pin*-layers are relatively free of traps, except for levels A at  $E_v + \sim 0,41\text{eV}$  and B at  $E_v + \sim 0,68\text{eV}$ , present in concentrations of  $5 \times 10^{13} - 5 \times 10^{15} \text{ cm}^{-3}$ . These two deep acceptor levels determine the minority carrier (hole) -lifetime and reverse recovery time of rectifiers, respectively. The concentration of A and B traps have influence on the width of *i*-region and the location of *pin* junction in epitaxial layer also. The physical nature of the A and B traps is still the subject of debate. It is known that A and B centers are observed in a number of layers of GaAs, grown by liquid phase epitaxy in a hydrogen atmosphere. Various sources have considerable variations in the ionization energy and capture cross sections. Perhaps this variation is due to different growing conditions [1]. The authors of [2] using the results of photoemission measurements concluded that A and B levels communicate with two different charge states of isolated GaAs antisite defect. Afterwards this has been proved [3] and suggested that these levels correspond to different complexes of defects including Ga<sub>As</sub> antisite defect. However the Zn diffusion process in some way getters or destroys the A and B levels, as mentioned in [4]. The study of the background spectrum of the deep levels that are centred in the base areas of *pin* structures is the main goal of the present paper.

## 2 Materials and methodology

The study of  $p^+ - pin - n^+$  structures was carried out in terms of their technological anonymous origin. The structure manufacturer provided only general manufacturing process data. Specific technological nuances of their production remained are not disclosed. This was done advisedly in order to maximize the objectivity of the results and conclusions.

The schematic picture of  $p^+ - pin - n^+$  structures used in experiments is shown in Fig. 1.



Figure 1: Scheme of GaAs  $p^+ - pin - n^+$  structure.

The investigated structures were prepared as follows. The  $p^+pin-n^+$  structures were grown on  $p^+$  GaAs substrates doped up to  $N_a = 10^{18} \text{ cm}^{-3}$  by liquid-phase epitaxy (LPE) [5]. The donor concentration in the  $n^+$  layer was  $N_d = 10^{18} \text{ cm}^{-3}$ . Ohmic contacts were deposited on the  $p^+$ - and  $n^+$ - surfaces: Ni+Ag and Au+Ge+Ag respectively. The structures were formed on wafers of the standard diameter, and then the wafers were separated into chips of  $3 \times 3 \text{ mm}^2$ . Three groups of structures were studied which differed in their manufacturing techniques: Group I, Group II and Group III. During the study, the current-voltage (I-V) and capacitance-voltage (C-V) characteristics, and their temperature dependence were measured. Spectra of deep levels were investigated by the capacity relaxation method. Also were measured the dynamic turn-off characteristics. For the measurements, the following basic equipment was used: Agilent B1500A Semiconductor Device Analyzer, Deep Level Transient Spectroscopy DLS-83D, Dynamic Parameter System LEMSYS DMS.

In a number of capacitance-voltage measurements was used extra lighting by white LED with radiant flux 1.5 mW.

In analyzing the results for all samples were kept the unified methodological approaches that have been well developed in number of publications, for example [6–8] structures is the main goal of the present paper.

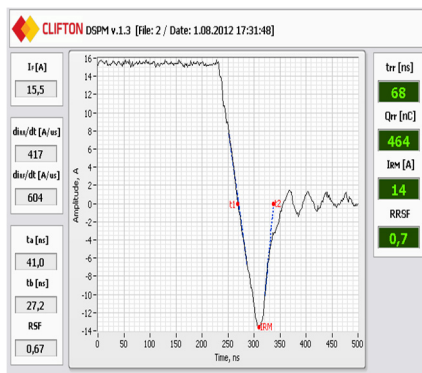
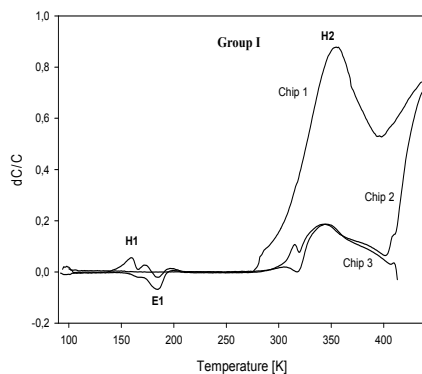
### 3 Results and discussion

To ensure the reliability of statistical significance a great number (about 100 pc.) of chips were provided for an experiment. Chips were divided into groups according to their technological features of production. Figure 2 shows the temperature DLTS spectra of the background deep levels for the samples from the three groups of structures. In parallel are presented turn-off characteristics, which are typical for chips belonging to the corresponding group.

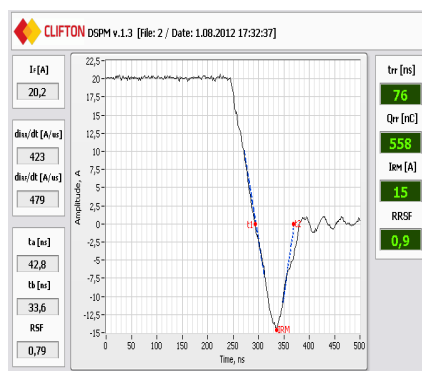
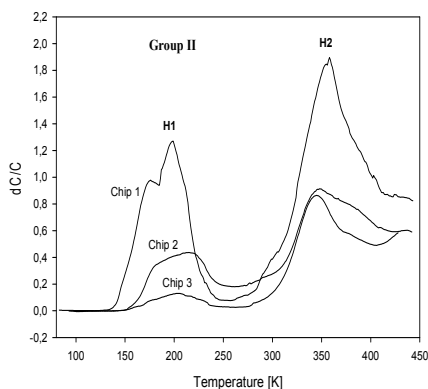
It should be noted that the comparative evaluation of the spectra were performed at a qualitative level. The Lang method, proposed in [6], can be applied uniquely for Schottky diodes or for structures with sharp  $pn$  junctions. In the investigated pin structures the applied external voltage is, in reality, focused on the  $i$  layer and weakly modulates the expansion of the space charge in the  $p$  and  $n$  layers by changes in the diffusion potential.

From the obtained DLTS spectra, it is impossible to calculate the energy levels depth, their concentration, and the capture cross section, and, therefore, to identify them.

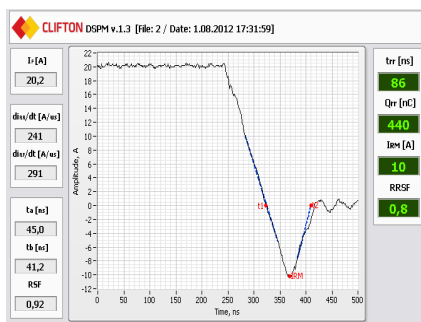
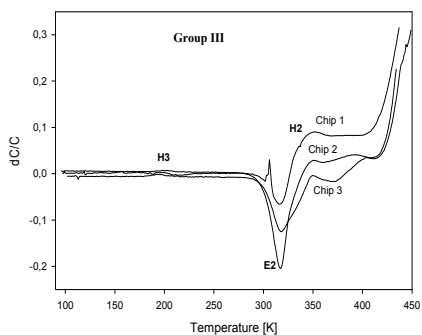
The presented spectra shows the presence of hole and electron type deep levels in all samples. Depending on the technology variants, the spectra of background defects have different configurations. However, within each group of samples the configuration of the spectra is similar. At the same time the chips having identical configurations of DLTS spectra show reverse recovery times ( $t_{rr}$ ) in intervals typical for corresponding groups (see Fig. 2).



(a)



(b)



(c)

Figure 2: Temperature spectrum of deep levels in  $p^+pin-n^+$  structures (left) (reverse bias  $U_r=-10V$ , filling pulse  $U_f=1V$ , frequency  $f=500Hz$ , and related turn-off characteristics for (a) Group I; (b) Group II; (c) Group III).

Ensembles of defects with similar energy parameters lead to distortion of the peaks as well as their splitting, which adds to the difficulty in identifying them. It is also essential that all three groups in the range of 350 K stable demonstrate the hole trap H2. In earlier studies, for example [9–14], in addition to background defects in the pin layers grown by LPE, typical hole traps A and B are present with activation energies  $E_v = +0.41$  eV and  $E_v = +0.68$  eV, respectively.

This knowledge allows us to correlate the peak of H<sub>2</sub> with B center because the activation energy for this peak, determined from the  $p^+pin-n^+$  spectra, is (+0.530 eV ÷ +0.681 eV). Trap A with a more shallow level cannot be defined being “shadowed” by the background impurities.

The temperature changes of the C-V characteristics of the  $p^+pin-n^+$  structures showed strong dependence of the capacitance on the temperature (Fig. 3).

As shown in Fig. 4 the concentration of ionized levels and built-in voltage defined from the C-V characteristics also depend on the temperature.

Using the method proposed in [15] we can pick out the total concentration of deep levels in the band gap. As seen from the DLTS spectra (Fig. 2), at temperatures above 400 K and below 100 K, deep levels are not fixed. This means that at  $T > 400$  K the steady filling of deep levels has time to follow the filling pulse, but at  $T < 100$  K the initial deep levels filling is stored. Hence, the difference  $N_{dop(400K)} - N_{dop(100K)}$  will give us the total concentration of deep levels ( $N_t$ ) in the band gap. For the three groups of structures, the following

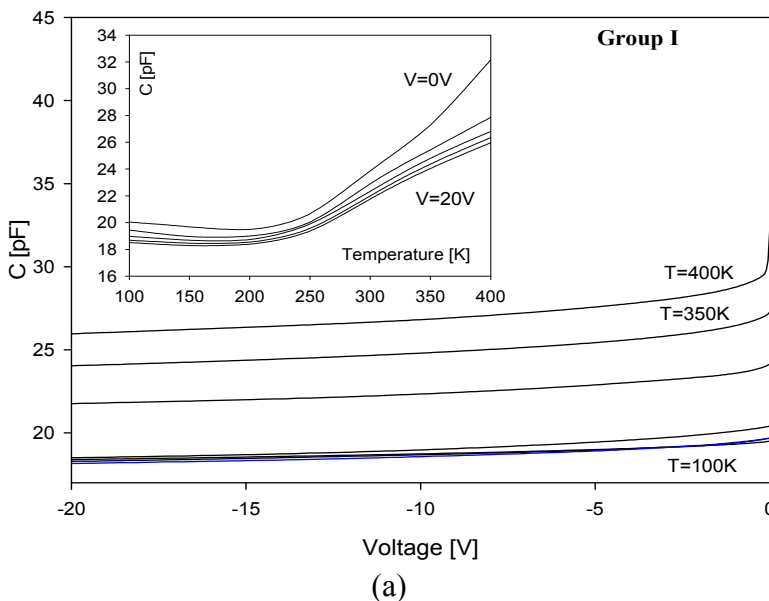


Figure 3: The dependence of the capacitance-voltage characteristics and the stationary capacitance on the temperature for (a) Group I; (b) Group II; (c) Group III.

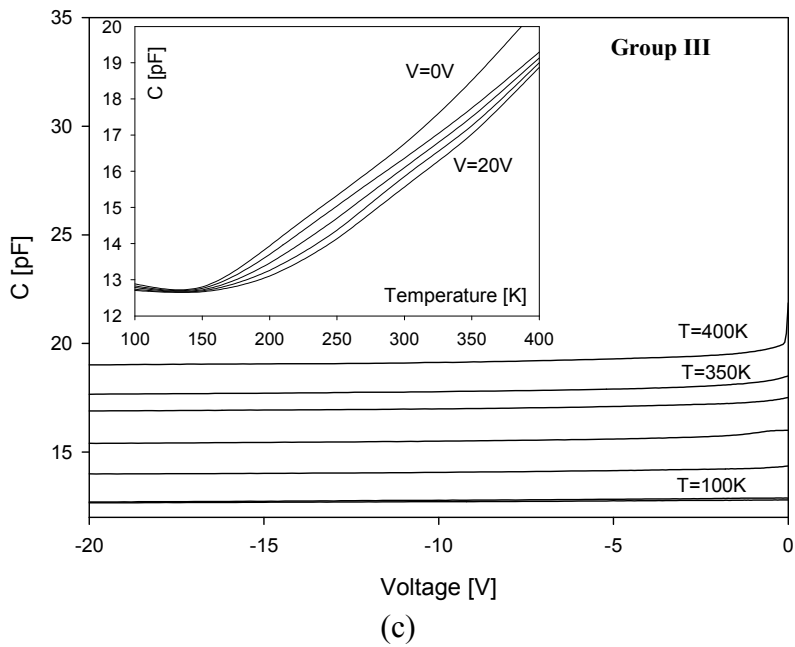
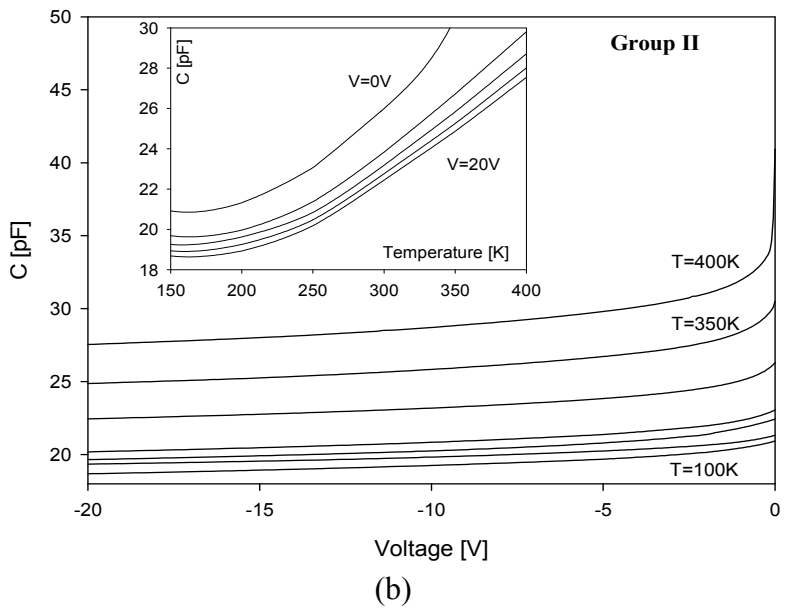
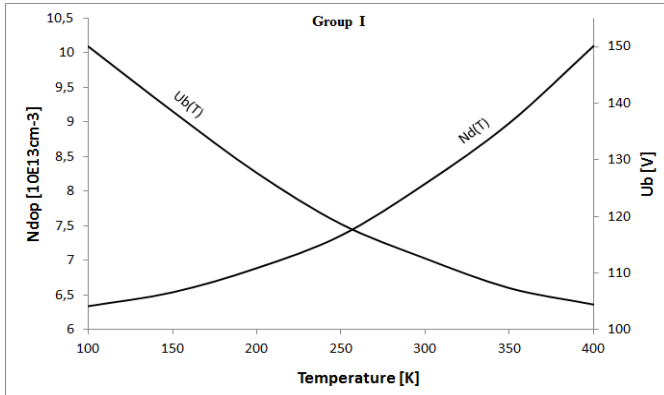
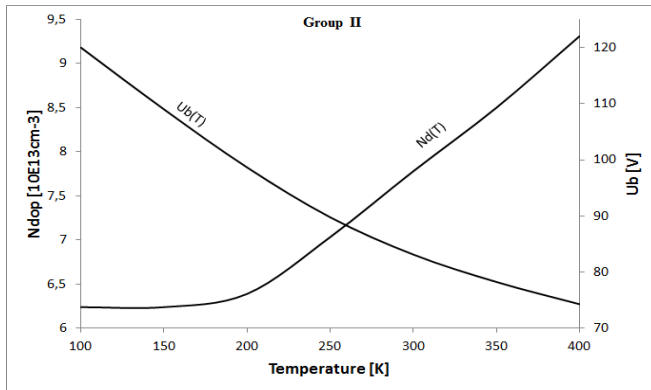


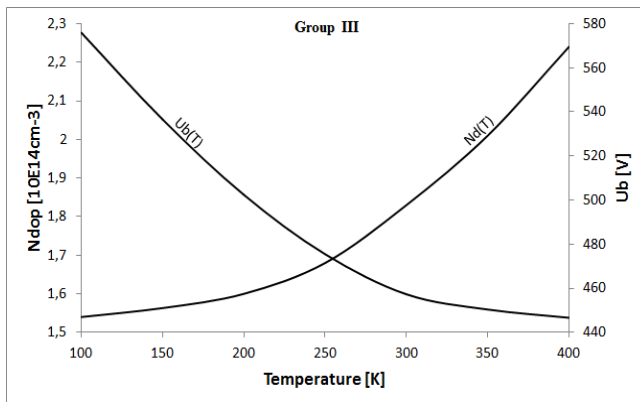
Figure 3: Continued.



(a)



(b)



(c)

Figure 4: The temperature dependence of the concentration of ionized levels ( $N_{dop}$ ) and built-in voltage ( $U_b$ ) for (a) Group I; (b) Group II; (c) Group III.

concentrations of deep levels were obtained: Group I  $N_t = 4.66 \times 10^{13} \text{ cm}^{-3}$ , Group II  $N_t = 3.07 \times 10^{13} \text{ cm}^{-3}$ , Group III  $N_t = 7.0 \times 10^{13} \text{ cm}^{-3}$ .

It can be seen that the concentration of the deep levels in the structures is comparable with the concentration of shallow impurities (see Fig. 4) and, therefore, the deep levels play an active role in the compensation of the layers grown in the LPE. As a result, structures are characterized by a sufficiently wide  $i$  region. The  $i$  layer, measured by the electro optical method, for all the structures in the three groups is  $30 \pm 5 \text{ } \mu\text{m}$  wide. As shown in Fig. 3, the structures of all three groups are characterized by strong dependence of the C-V characteristics on the temperature. With a set of formulas of the thermionic emission model barrier capacitance, the width of the space charge, the built-in (diffusion) potential, and the total concentration of impurities:

$$C = \frac{\varepsilon \varepsilon_0}{w} A \quad (1)$$

$$w_0 = \sqrt{\frac{2\varepsilon \varepsilon_0 (\phi_M - \phi_S)}{Nq^2}} \quad (2)$$

$$qU_B = \phi_b - (E_C - E_{F_n}) \quad (3)$$

where  $C$  is the barrier capacitance,  $\varepsilon$  the dielectric permittivity,  $\varepsilon_0$  the electric constant,  $A$  the area of the junction,  $w$  the width of the space charge,  $U_B$  the diffusion voltage,  $U_R$  the reverse bias,  $q$  the elementary charge,  $N_{dop}$  the impurity concentration,  $\phi_b$  the barrier height,  $E_C$  the bottom of the conduction band,  $E_{F_n}$  the Fermi level, we can carry out an analytical study of the experimental dependencies.

First, it should be noted that the width of the space charge calculated by Eq. (1) and Eq. (2) are almost the same in magnitude. This means that the junction active area of the structure is the same as the chip area, so the technological errors of the formation of the junction, and by the surface metallization can be avoided. The first conclusion to be drawn from these results is that the space charge region at zero bias, even at 400 K, completely overlaps the  $i$  layer ( $\sim 30 \text{ } \mu\text{m}$ ), and spreads into the  $p$  and  $n$  depletion layers. This means that in the recharge process, two interfaces, the  $p$ - $i$  and  $i$ - $n$  regions, can be affected, which in turn does not allow a monosemantic interpretation of the spectra in accordance with the Lang model. Ignoring the temperature dependence of the dielectric constant in  $C(t) = \frac{\varepsilon A}{w(t)}$ ,  $C_{(400K)}/C_{(100K)}$  must be equal to  $w_{(100K)}/w_{(400K)}$ . In turn, the width of the space charge depends on the built-in voltage (thus the diffusion potential) as  $w(U_B) \propto U_B^{1/2}$  (Eqs 2, 3). The ratio  $w_{(100K)}/w_{(400K)}$  for different groups is  $1.4 \div 1.57$ , while  $U_B^{1/2}_{(100K)}/U_B^{1/2}_{(400K)}$  changes only as  $1.1 \div 1.27$ . Therefore, the main role in the temperature change of the capacitance is in changing the cumulative concentration of the impurities and defects, which in turn indicates evidence of an overcompensated layer in the base region of the structures.

These considerations are also supported by the I-V temperature dependence (see Fig. 5).



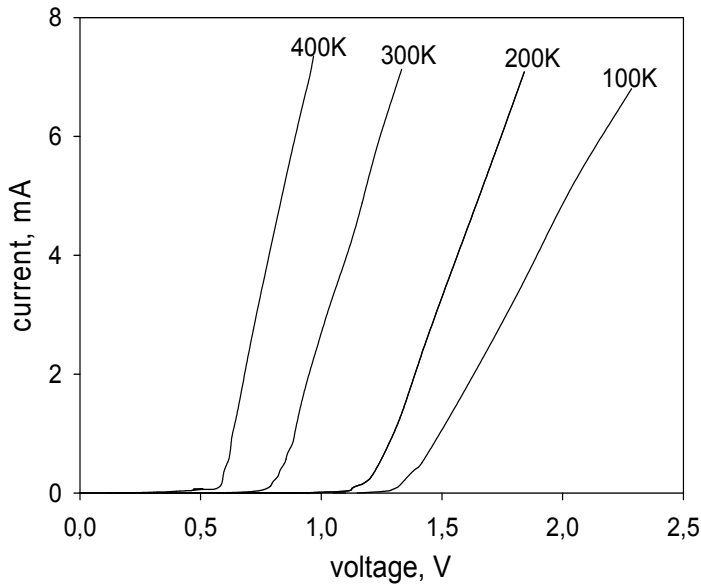


Figure 5: Typical I-V temperature dependence for GaAs  $p^+pin-n^+$  structures.

The resistance of the diode structure increases significantly at temperatures below 200 K. Permanent changes in the capacitance in all the temperature range suggests that the width of the overcompensated layer practically coincides with the width of the space charge region. A very weak change in the capacitance, at least in the range  $1\text{ V} < U_R < 20\text{ V}$ , confirms the primary impact of deep levels and the evidence of a homogeneous spatial distribution of defects across the width of the space charge.

When using the backlight when measuring the C-V characteristics for  $p^+pin-n^+$  structures it causes an increase in capacity at all temperatures. Capacitance-voltage characteristics obtained in the dark and under illumination shift up paralleled themselves (see Fig. 6).

The reason for increased capacity under illumination may be a decrease in the width of the space charge region due to activation, when illuminated, interface states at the junction borders in the structure [15, 16].

## 4 Conclusion

The DLTS spectra obtained from the analyzed  $p^+pin-n^+$  structures demonstrate the presence of electron and hole type deep levels in all investigated samples. However, their common feedbacks give different configurations of the DLTS

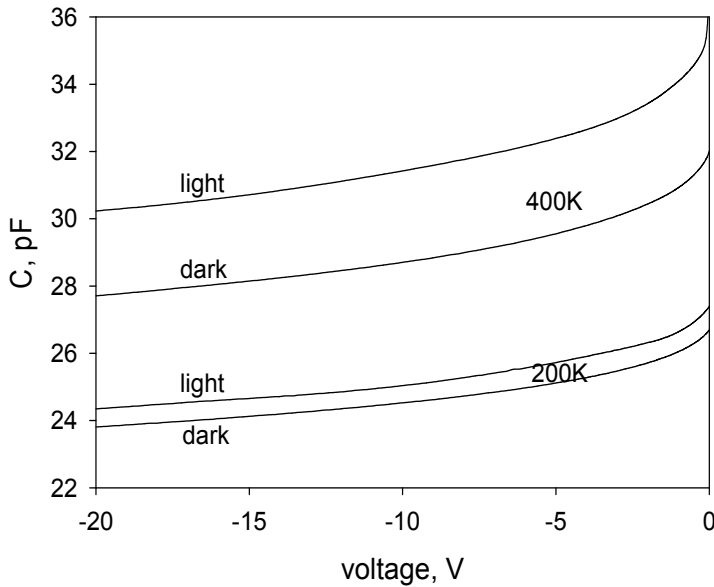


Figure 6: The shift up of C-V under illumination at 200 K and 400 K.

spectra. Nevertheless within each group, the configuration of the spectra is similar. And for each configuration correspond a certain set of output parameter characteristic; for example such as turn-off curves (see Fig. 2). This indicates that the sources of defects are stable, reproducible and depend on the variations in epitaxial growth technology. The width of the space charge calculated from the C-V characteristic exceeds the width of the  $i$  layer and can spread into the  $p$  and  $n$  depletion regions. The permanent change in the capacitance over all the temperature range and the very weak dependence of the capacitance on the reverse voltage indicate that the thickness of the overcompensated layer practically coincides with the thickness of the space charge, as well as indicating evidence of a homogeneous spatial distribution of defects across the width of the space charge.

The fact that, in the general spectra for all three groups, the steady presence of hole traps, such as the center of H2 (Fig. 2), can be identified as significant. This means that from the special studies on the “proper” test samples made from the  $p^+pin-n^+$  structures, for example, the Schottky diode, or a sharp  $pn$ -junction, the exact parameters of the key defects (centers A and B) can be set. Then, the correction factors for the peaks of interest in the general background spectra of  $p^+pin-n^+$  structures can be determined. This in turn will provide an opportunity for express DLTS control of the finished product and thus can be realized in on-line monitoring of the LPE process in order to optimize the dynamic characteristics of the devices.

In addition to that, there is hope that on the basis of more precise information about the structure of the deep levels, their concentration and capture cross

sections we will have a more reliable source of data base to build a formal model of the existing pin structure. And this in turn means that during the design phase of diode structures with the required output parameters, we can use the methods of computer simulation, the use of which for the moment does not give good results because of uncertainty of situation in pin region of diodes.

## Acknowledgements

This research was supported by the European Union through the European Regional Development Fund, Nations Support Program for the ICT in Higher Education “Tiger University”, the Estonian Research Council under research projects SF0140061s12, ETF8592, and IUT19-11, and the Foundation Archimedes through the Centre of Excellence CEBE (TK05U01) for supporting the technology oriented scientific projects in Estonia.

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