Characterization of deep level traps in semiconductor structures using numerical experiments

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Abstract

Deep level traps in the forbidden bandgap of semiconductor can be either a desired effect or technological harm that should be avoided. Understanding the essence of specific deep traps, their influence on electrical optical and mechanical characteristics of devices and circuits makes it possible to drive the manufacturing processes to maximize the desired effect. Deep level transient spectroscopy (DLTS) is one of the traditional methods for finding the trap levels in the semiconductor possible energy level bands. Majority carrier trap levels, concentrations and even location in the structure can be extracted from DLTS measurements. Finding parameter values for minority carriers is more complicated and needs extra efforts, combining DLTS with other measurements. Although DLTS, and its more advanced flavors like Laplace DLTS, can be utilized to measure trap parameters in semiconductors with high sensitivity, they do not determine the essence of the trap. Numerical simulations can be used to verify the influence of defect parameters on characteristics that are measured during DLTS. The simulation results and the DLTS measurement results carried out at the Thomas Johann Seebeck Department of Electronics are compared and discussed.
Keywords: numerical simulation, deep level traps, GaAs PiN diode.

1 Introduction

Semiconductor devices operating at high speed, high power and high temperature have been the challenges for many decades after their first


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appearance in the middle of the last century. Most conventional semiconductor power devices have been formed using silicon (Si). Due to the maturity of the use of Si, the performance of conventional power diodes to carry high currents and block high voltages is approaching the theoretical limit for Si. There are many applications, like electric motor control, power supplies, lightning protection of lines and equipment - not to mention traditional power generation, conversion and transmission that could benefit from devices with higher capabilities.

Wide band gap semiconductors such as diamond (C), silicon carbide (SiC) and gallium nitride (GaN) are the promising materials for new power or optical devices and theoretically they should bridge the gap between the material limitations and application demands for higher frequencies and higher blocking voltages. Unfortunately, the real application of the devices based on wide band gap semiconductors has still strongly limited due to specific crystal growth quality problems and other device manufacturing difficulties.

In the power electronics industry we see Si still strongly represented, SiC and GaAs as niche players (from which SiC is predicted to be growing quicker) and C as a new most fast emerging materials, still staying in the shade of SiC. There is also development for the acquisition of GaN into new developments.

During over 50 years of development it seems that nearly all usable ideas in the field of power device build-up physical principles have been utilized. Modelling and simulation of devices has always had a significant role in the development of devices, explaining the behaviour and improving geometrical structure, based on the underlying physics and models using simplifications to the extent that still depicts the real life correctly. Lately, more and more attention has been paid to large bandgap semiconductors for the needs in space and communication technology (RF speed and radiation proof requirements) but also due to the fast development of automotive industry and the need for high-current high-temperature resistant materials. A lot of problems in numerical simulation are inherited from the legacy of Si-optimized simulations – normalization of parameters, lower spread of doping and current densities, solution convergence criteria, etc. Most of parameter values needed for simulation of new materials can be found in general reviews and are implemented in commercial simulators when selecting device material. One of the significant differences between Si and wide bandgap semiconductors is the behaviour of impurities. To model the deep level traps and defects the modified Poisson's equation is used:

$$div(\varepsilon \nabla \psi) = q(n - p - N_D^+ + N_A^-) - Q_T \tag{1}$$

where ε is the permittivity, ψ is the potential, q is the electron charge, n and p are charge carriers, and N_{D+} and N_{A-} are ionized impurity concentrations, respectively, and Q_T describes the charge due to traps and defects. The latter is calculated taking into account the densities of ionized donor-like and acceptor-like traps. Carriers being emitted or captured by the donor and acceptor-like traps are accounted by modifying the Shockley-Read-Hall (SRH) recombination rate in the carrier continuity equations. The enhancement factor takes into account the probability of tunnelling process, including barrier lowering, as well.

Most commonly two methods, thermal admittance spectroscopy (AS) and deep level transient spectroscopy (DLTS) are used to derive the values of ionization energy and capture cross sections from experimental data.

Thermal admittance spectroscopy (AS) is a subset of impedance spectroscopy. The method operates applying reverse voltage with comparatively small AC signal (compared to kT/q) to a simple structure with depleted region (pn or Schottky diodes) and measuring conductance and/or capacitance on several different frequencies.

The impurity ionization energy (or the impurity emission rate) and the carrier capture cross section are derived from the Arrhenius plots of the measured data. It has been notified, that the derivation of several temperature-dependent parameters from one 1D experimental dataset might not be accurate and hence a 2D Arrhenius plot method has been proposed [1].

Deep level transient spectroscopy (DLTS), as reflected in the method name, is based on the measurements of transient process parameters while sweeping temperature or pulse frequency. From the measured capacitance, current or charge transient curves on different temperatures, using the concept of rate window introduced by Lang [2], maximums in decaying waveform are extracted. To get rid of noise, the signal is multiplied with reference signal, equipment specific weighting function and the after that filtered. From the subsequent products (through Arrhenius plot), trap level, density and capture cross section can be derived. The method works for majority carriers, for minority carriers' additional optical excitation is needed. The first DLTS measurement sets included double-boxcar or lock-in amplifier equipment. Further developments included waveform digitation and following flexible signal processing possibilities. The most significant step in energy resolution and low defect density measurements has been the invention of Laplace deep level transient spectroscopy (LDLTS) in 1993 by L. Dobaczewski, I. D. Hawkins and A. R. Peaker.

The Thomas Johann Seebeck Department of Electronics owns the computer controlled deep level spectrometer DLS-83D (Semilab Inc., Hungary). It is a capacitance transient lock-in amplifier measurement station with the capabilities of C-V and I-V measurements + Arrhenius plots. The temperature controller and measurement sideward could be feasible for implementation for AS measurements. Laplace DLTS measurement station is in the process of implementation.

2 Experimental part and simulations

The experimental part that the numerical simulations are based on the *PiN* diode deep level traps measurements at the Thomas J Seebeck Institute of Electronics. The experimental diodes came in 3 different doping profile groups. The profile shapes without numerical data are depicted in Fig. 1. The exact numerical data was used during the simulations but is not public information.

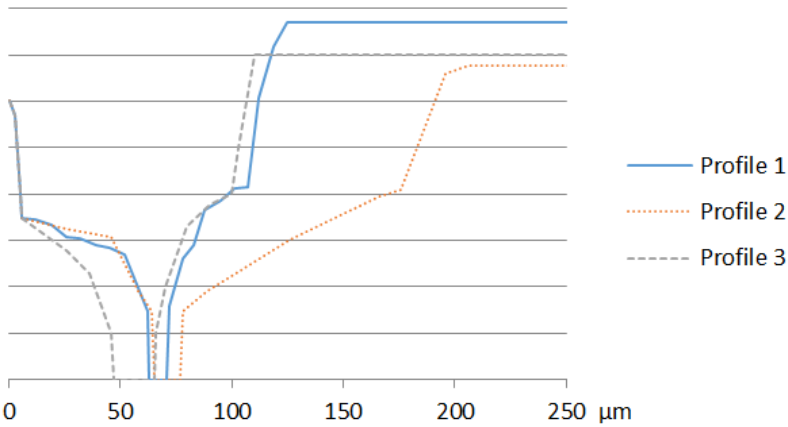

Figure 1: Doping profiles for the three investigated device groups. Profile 1 corresponding to group 1, profile 2 to group 2 and profile 3 to group 3.

During the study of the samples the current-voltage (*I-V*), capacitance-voltage (*C-V*) and their temperature dependence was measured. The spectra of deep levels was investigated by the capacity relaxation method (DLTS).

The difficulties of DLTS investigations rise from the structure of the *PiN* diode, having two sequential junctions – n^{+}->*i* and *i*->*p*. The DLTS methodology is well established for Schottky diode type device measurements (majority carrier traps) and *pn*-diode type device measurements, not for devices having more than 1 junction. Therefore the measurements were carried out in three series – starting with overall *PiN* diode deep level spectrum measurements and continuing with measurements in *n-i* layer and *p*-layer.

Numerical simulations of the whole *PiN* device are still continuing, for investigation and verification of the assumptions and conclusions.

The DLTS measurements revealed that deep traps are present in all 3 groups of sample diodes. Two deep levels, HL" (also known as B-centre) and HL5/known as A-centre) are always present in epilayers manufactured using LPE technology.

2.1 Space charge region

From experimental *C-V* characteristics it was calculated [3] that the space charge region width exceeds the *i*-layer width and spreads into p^{-} and n^{-} depletion layers. In this way the recharge process affects both interfaces, *n-i* and *i-p*, which causes error when the measured DLTS spectra is tried to fit directly to the Lang model. This find is supported by the simulation results. In Figs 2 and 4 (respectively for temperatures 200K and 400K) is seen, that charge is concentrated deep in *n* area, giving unexpected 2-peak phenomenon in the area where the concentration of the n-doping reaches the overcompensated *p*-doping concentration level of the *i*-area. The simulated carrier concentrations for the same temperatures (Figs 3 and 5) support the abovementioned finding.

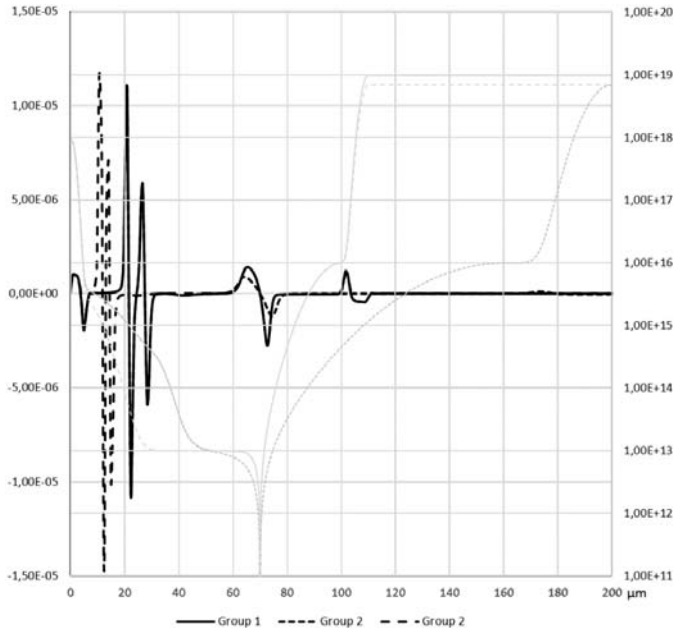

Figure 2: Electric charge spatial distribution characteristics simulations for all device groups at temperature 200K. Doping profile data in light gray.

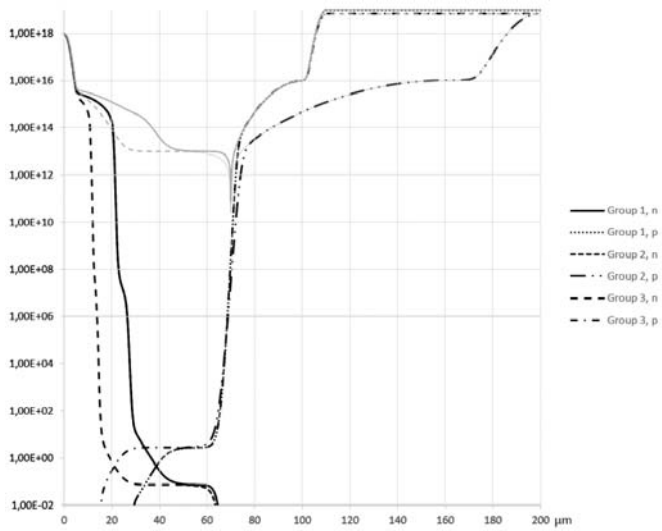

Figure 3: Carrier concentration distribution characteristics simulations for all device groups at temperature 200K. Doping profile data in light gray.

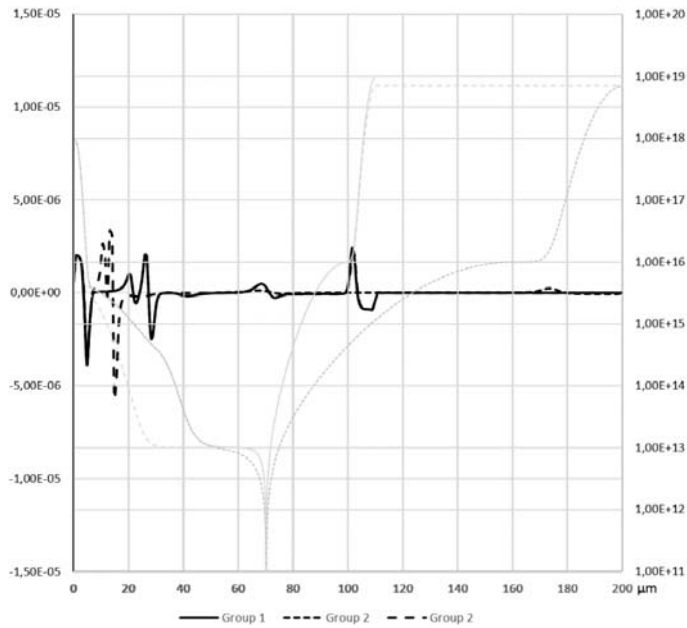

Figure 4: Electric charge spatial distribution characteristics simulations for all device groups at temperature 400K. Doping profile data in light gray.

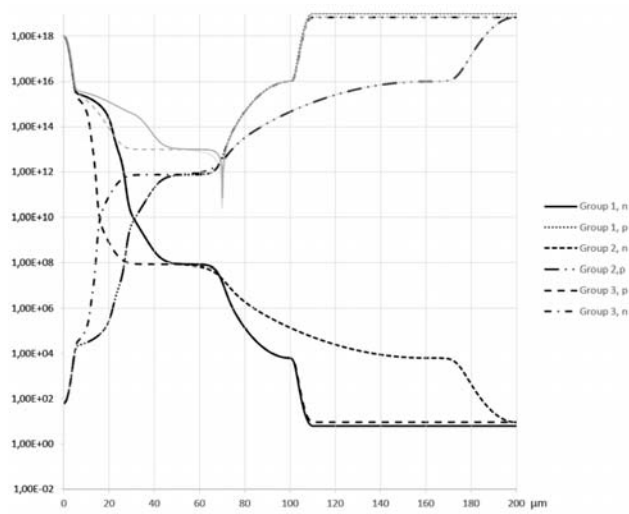

Figure 5: Carrier concentration distribution characteristics simulations for all device groups at temperature 400K. Doping profile data in light gray.

2.2 DLTS spectrums

During the measurements two hole-type traps have been introduced by the diode manufacturing technology. 1 electron trap, EL2. The nature of EL2 is unclear, is observed at crystallization temperatures above 850°C. Hole traps A and B are always present, not dependent on crystallization temperature – but the formation of *i*-layer takes place only at temperatures above 850°C. Due to the energy level proximities between the levels there should be some interaction between them (mutual partial gettering) it is supposed that the EL2 level can act as a control engine for A and B centres in the *i*-region of GaAs *PiN* structures.

Simulated DLTS characteristics for devices belonging to the 3 different groups are depicted in Fig. 6. Corresponding measured characteristics are depicted on Fig. 7. Although there is a similarity in the form of the goup characteristics, the trap maximums are shifted by approximately 50K.

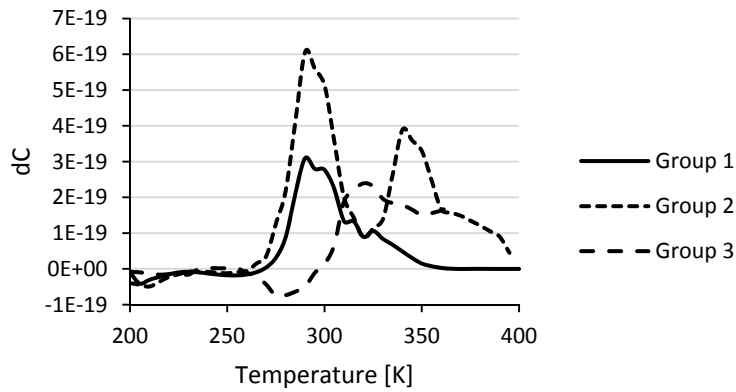

Figure 6: DLTS spectrum simulation results for devices from groups I–III.

2.3 Conclusion

Space charge from simulation does not coincide the conclusion drawn from experimental result. The peaks of DLTS signal and simulated DLTS signal differ on the temperature scale. This might be the result of different techniques for DLTS signal acquisition – measurements carried out with DLTS83 measurement station, using the lock-in amplifier approach and simulations – using the double boxcar approach. Also, during simulations the interaction of levels is not implemented in the models – assuming simple cumulating of effects resulting from different levels. Better fit for the space charge distribution and/or DLTS simulated results could be achieved with uneven distribution and density of traps. Still, the overall similarity in DLTS signal shapes supports the idea of the possibility to evaluate the quality of devices based on DLTS measurements. Instead of temperature sweep frequency sweep at constant temperature should be used instead of temperature sweep at constant measuring pulse frequency.

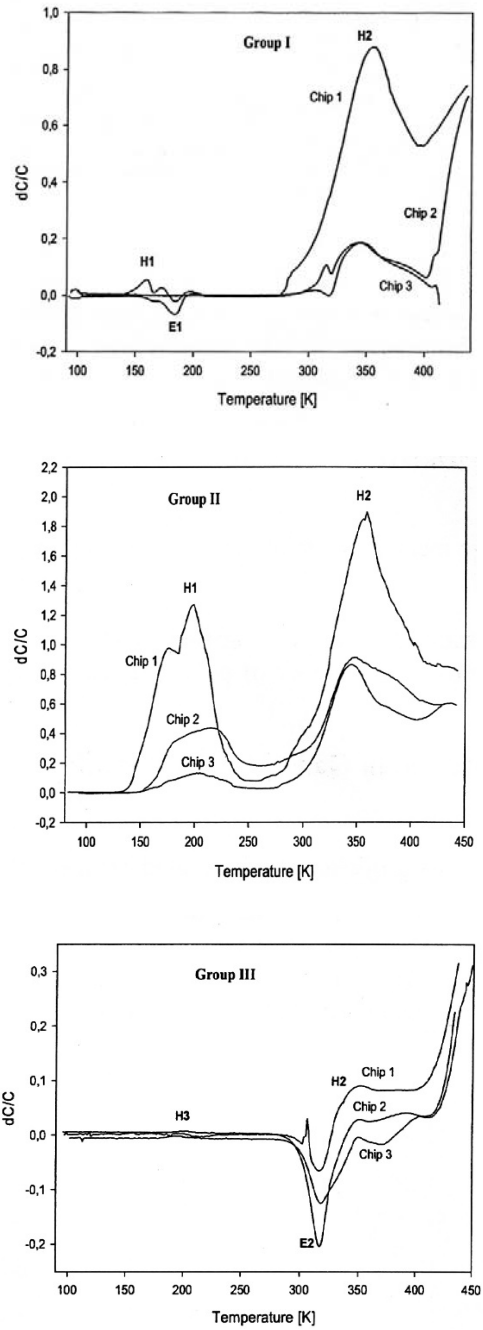

Figure 7: Measured DLTS spectrums for devices from groups I–III.

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