Characterization of the temperature dependent behavior of snappy phenomenon by the switching-off of GaAs power diode structures

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Abstract

Power semiconductor devices are facing different failure mechanisms which limit the safe operating area of these devices. Two different mechanisms influence the thermal behaviour of power devices, first the ambient temperature, and secondly self-heating phenomenon described traditionally over the lattice thermal behaviour model. It is demonstrated in different published materials how the device internal processes can be investigated by means of device numerical simulation procedure. In our paper we focus on the numerical analysis of GaAs based power pin structures applied for detection of anomalies in the switching process of devices taking into account the influence of ambient temperature amplified by the self-heating phenomenon introduced over the lattice thermal model. Due to the fact that the switch-off of power diode structures is one of most critical acts in different power converters, like for example DC/DC converters, we put our focus on the exact thermal description of the devices under the switching process. Special effort has been taken for the situations, where during the switching process the total thermal situation leads the device close to the thermal breakdown instead of normal electrical breakdown. The influence of current crowding plasma generation near the metallic contacts seems to take place. The smooth snappy switching characteristics behaviour and it's mechanism under the temperature influence is simulated and the results are presented. Examples on current destabilizing effects in the switching process and the limitations of switching current detected from the device simulation are discussed.

Keywords: GaAs power devices, numerical simulation, temperature influence, self-heating phenomenon, switching properties, snappy effect.

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1 Introduction

Over the last decades we have been the witnesses of trend for reducing the power losses in power semiconductor devices together with another trend for increasing the power density and minimizing the power consumption of the devices inside the power converters and transducers. Both trends lead us to strong scaling down of the chip geometry and increasing the current density through the devices itself. Higher operating temperatures up to 200°C or even 400°C are an important path to enhanced power density. Therefore the requirements concerning reliability and ruggedness in the application are more important than ever before. Concepts to ensure or even enhance the critical behaviour have a crucial issue already in the early design stage of new power devices. Understanding the limiting factors influencing the critical thermal behaviour of power devices under the turn-off process and the mechanisms that may lead to their destruction is the task of this paper, where the numerical experiment has chosen as a tool for getting the results in case of simultaneous influence of ambient temperature and lattice self-heating phenomenon on behaviour of switching properties of GaAs power *pin*-diode structures.

Certain number of publications, e.g. [1–4] gives the explanation of reasons and the ultimate goal of the predictive numerical experiments for detection of the limits of robustness, but unfortunately the processes are in many aspects still unclear. The influence of different physical effects like avalanche impact ionization, high current density, high electric-field strengths, self-heating, or the effects of parasitic (e.g. unsymmetrical current distribution or current crowding effect in device structures) effects could be investigated in a most effective way using numerical experiments. High power density resulting in homogeneous or inhomogeneous over temperature regions inside the structure and it can introduce a number of distributed local effects like avalanche breakdown, dynamic increase of electric field during switching at high current density, or thermal runaway at high temperature. Today, majority of these effects can be understood much better using exact enough numerical simulation procedures.
In order to reduce the losses in power converters, involving *pin*- or Schottky diode structures or high voltage stacks, semi-wide bandgap materials (e.g. GaAs) based device structures have been introduced. Typically the cost-competitive manufacturing technology uses the Liquid Phase Epitaxy (LPE) solution (e.g. [5–7]), and the analysis of electrical characteristics under different ambient conditions have been carried out using numerical experiments (e.g. [8–9]).

Due to the fact that the switch-off of power diode structures is one of most critical act in different power converters, like for example DC/DC converters, we put our focus on exact thermal describing of the devices under the switching process. Special effort has been taken for the situations, where during the switching process the total thermal situation leads the device close to the thermal breakdown instead of normal electrical breakdown. The influence of current crowding plasma generation near the metallic contacts seems to take place. The smooth snappy switching characteristics behaviour and it's mechanism under the temperature influence is simulated and the results are presented. Examples on

current destabilizing effects in switching process and the limitations of switching current detected from the device simulation are discussed. By means of numerical simulations the causes for the temperature-dependent performance of the cell are discussed.

2 The problem

For GaAs pin-device structures show sometimes by the switch-off process strange behaviour of the reverse recovery characteristics and such behaviour is well-known as a snappy process or behaviour. If at room temperatures in major cases such behaviour could be explained by the inaccurate measurement problem, then under higher ambient temperatures, the complexity of problem increases significantly, because the additionally introduced influence of self-heating phenomenon which transposes the problem into the volume of the device itself. Therefore for the numerical analysis of switching properties of GaAs device under high ambient temperatures the heat-flow and accompanying self-heating has to be taken into account. Additionally it is important to fix the fact that the thermal conductivity itself depends on temperature as well [e.g. 10] and for GaAs the temperature dependence exponent value is close to 1.25. So, if therefore, for a specific device it has been found that self-heating is relevant, then it is also relevant to take the temperature dependence of κ into account.

Our problem concludes not directly from the previous mentioned detail, but from the observations made by the numerical experiments for static and dynamic behaviour of the experimental diode structure. Fig. 1 shows the analysed structure geometry taken from [11, 13].

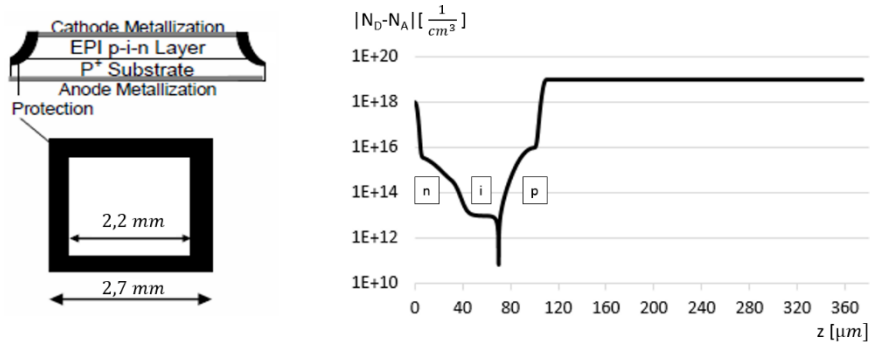
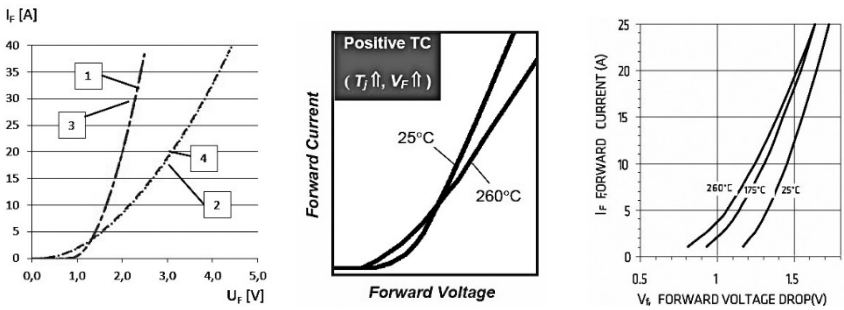


Figure 1: GaAs Diode Geometry [11] and doping profile.

The diodes are manufactured using Liquid Phase Epitaxy (LPE) technology [13]. The doping profile derived from an experimental diode and used for simulations is presented in Fig. 1.

The forward current I_F = 10A (corresponding current density would be 2.07 x 10^{-6} A/µm^2) with cathode dimensions 2.2mm x 2.2mm was assumed. For simplification, not a full device, but a smaller section is simulated. This approach

speeds up calculations but cuts possible edge effects (influence on leakage current and possibly breakdown). Reverse recovery can be simulated using ATLAS [12] device simulator inbuilt ramp voltage generator and distributed contact resistance. The challenge for modeling in device simulator is to achieve the initial 1A or 10A IF level, then ramp 200A/ μs. For simplification the series resistor value (R) to be used in simulations is chosen to be 1Ω. The self induction of the resistor plus measurement equipment added inductance (from wiring, contacts, etc.) is suggested to be kept low. The suggestion for finding target inductance value can be calculated as $L/R = t_{rr(min)}/10$, where $t_{rr(min)}$ is the minimal expected reverse recovery time of the diode. In our case, various simulations show reverse recovery time below 3 ns, hence the inductance value should be kept under 3×10^{-10} H. The simulations were carried out at room temperature 25°C and at maximal device operation temperature is given typically 260°C for GaAs devices.



(a) (b) (c)

Figure 2: Typical simulated forward voltage characteristics and the positive temperature coefficients (a). Line 1 and 3 – structure temperature 25°C, line 2 and 4 – structure temperature 260°C. Line 1 and 2 – i-region doping 1×10^{12}. Line 3 and 4 – i-region doping 1×10^{13}. (b) and (c) reproduced from commercial GaAs diode data leaflet [13] characteristics.

Comparing simulated structures and catalogue data, it is clearly seen that all simulated profiles reveal positive temperature coefficient on forward voltage, but in the same time the typical forward voltage from data leaflet in safe operating area (SOA) shows negative coefficient. So, the clear evidence of physical mismatch is presented, which is important to clarify before the analysis of switching properties, especially the claimed snappy behavior by the switch-off of the device. The behavior of simulated reverse characteristics does not show any unexpected behavior, as it is seen in Fig. 3, as well. The maximum held reverse voltage is higher than the measured values from the leaflets – that could be possibly explained by not taking account self-heating issue or differences in simulated and real doping profiles.

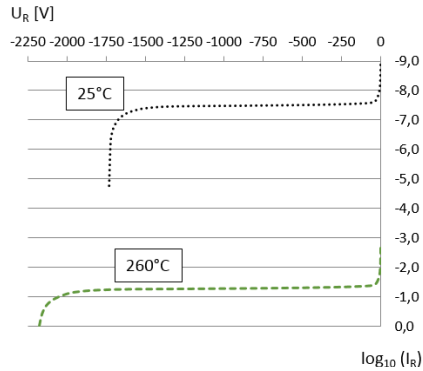
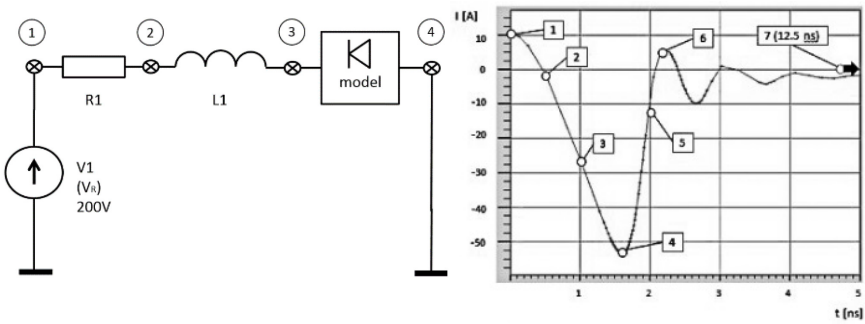


Figure 3: Simulated reverse characteristic at 25°C and 260°C.

For reverse recovery simulations for all diode profiles under investigation initial forward current 10A was chosen. For simulations a simple electrical schema was chosen, although more complicated circuit simulations were also tested but dropped due to simulations time and poor convergence reasons. Fig. 4 shows the simulated reverse switching characteristics at room temperature and our task is to clarify the influence of ambient temperature amplified by self-heating effect on this process.



(a) (b)

Figure 4: Simple circuit used for transient simulations (a). Typical transient result with snappy behavior, current versus switching time characteristic (b).

In most cases heat in semiconductor industry is applied either for initial device manufacturing or as post-processing to create protective oxide, or annealing out defects. The melting point of GaAs is 1511 K (1238°C). For growing GaAs single crystals, both Bridgman and Czochralski methods are applicable. In the hot zone the temperature is kept slightly above the melting point (ca 1240°C) while the seed (cold finger part) is at temperature 610–620°C. Rapid annealing (at temperatures 600–900°C during intervals usually less than

60 s) is used for improvement of device electrical characteristics after ion implantation. Rapid annealing is used additionally for improvement of electrical contact of the electrodes. The common process modeling tools from Silvaco and Synopsys recommend using temperature range 700-1400 C for simulating the diffusion or the annealing processes. It is generally known that heating GaAs above 700°C is hazardous due to vaporization of As from the material. The critical sublimation temperature for arsenic is reported to be around 900 K (627°C) [14, 15], although significant dissociation of the material begins at temperatures below 873 K (600°C).

3 Description of the method

The used numerical experiment bases on simulation environment, which takes into account the lattice heat flow and general thermal environments, and it accounts for Joule heating, heating, and cooling due to carrier generation and recombination, and the Peltier-Seebeck and the Thomson effects. The dependence of material and transport parameters on the lattice temperature is included as well. The lattice heat flow calculates taking into account the heat capacitance per unit volume, the thermal conductivity, the heat generation, and the local lattice temperature. Traditionally the temperature of holes T_p is set equal to lattice temperature T_L. The thermal conductivity k is material dependent and is generally defined as temperature dependent parameter, which might be incorrect, as we have seen already early in this paper. The basic band parameters are GaAs composition dependent. Low field mobility model is used and the electron affinities for GaAs in the given over the direction in k space. The density states (N_c and N_v) are each calculated from the effective masses definitions, and the bandgap narrowing effects are following the ideas presented in [16]. The lattice heat flow models originally developed at the Department of Electronics, Tallinn University of Technology [17] are integrated into the commercial simulator ATLAS by Silvaco. Heat flow equation is added to the fundamental set of semiconductor equations and solved consistently together.

4 Results and discussion

The first target for simulations was investigating the thermal effects at forward-biased device, reverse biased device (including breakdown) and transient process. The second target was to investigate the influence of temperature on changing the doping profiles inside the device and the following influence on the IVC and transient characteristics of the device.

During the simulations the highest lattice temperature observed with ambient temperature and anode heat sink at 260°C was 353°C what is significantly lower than the hazardous level (600°C and more). The only simulations exceeding the 600°C value were achievable with ambient temperature at 500°C – which is way out of the diode SOA.

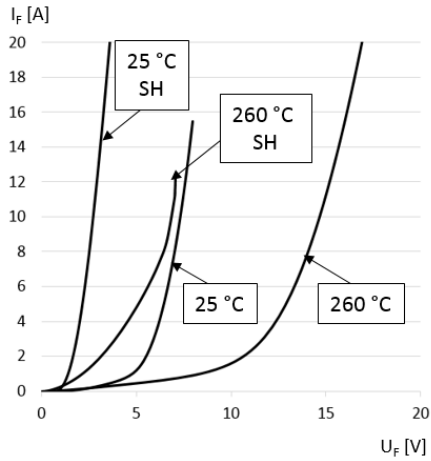


Figure 5: Forward IVC of simulated diode. Comparison of results with self-heating effect model (SH) included and excluded results at different ambient (and anode heat sink) temperatures.

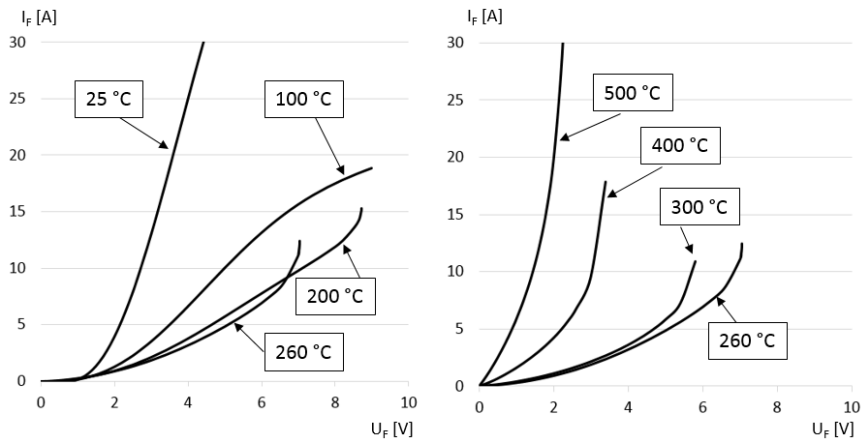


Figure 6: Forward IVC of simulated diode with self-heating effect model at different ambient (and anode heat sink) temperatures.

Transient simulation starts at 10A forward current that is subsequently ramped to reverse voltage bias -200V during 10^{-12} s. Current ramp comparable with measurement results were achieved by adding serial inductance to the simulated diode structure. The results of simulations at different temperatures are presented in Fig. 7. At lower temperatures the level of leaking currents is not

sufficient to heat the simulated device. At temperatures higher than 300°C leaking reverse current starts to heat the device but the influence is insufficient to cause device burnout (Fig. 8).

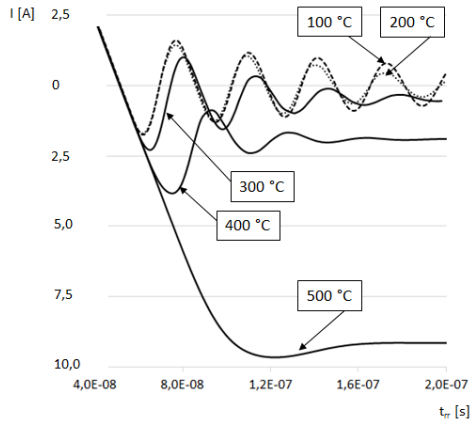


Figure 7: Transient simulation characteristics at different temperatures.

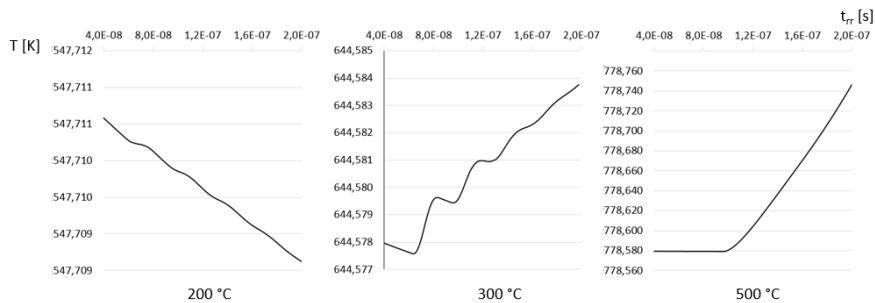


Figure 8: Mean temperature of the device during transient simulations.

The reverse characteristics of the simulated device reveals that till device temperatures up to 200°C the held reverse voltage value is acceptable. From 260°C the reverse voltage hold starts to drop rapidly (Fig. 9).

Deeper investigations of the reverse IV characteristics revealed that the electric field and generation of carriers was concentrated into the low-doped area. The high-doped anode and cathode areas were flooded with carriers to the extent where even sharp edges of contacts did not initiate destroying current spikes.

For investigating the influence of temperature on the doping profile of the device, the commercial, numerical 2-dimensional semiconductor process simulator Athena (Silvaco Co product) was used. Athena includes the possibilities of simulating different semiconductor materials (including GaAs) and different semiconductor industry processes (including diffusion and

annealing). The simulations showed that there is no significant diffusion of Si (if filling the Ga sites in the lattice acts as donor and if filling the As sites in the lattice acts as acceptor) at temperatures below 700°C. The simulation results are presented in Fig. 10. Annealing the device structure for 416 days was simulated at temperatures 260°C, 700°C, 900°C, 1000°C, 1100°C and 1200°C. The results show that semiconductor industry process simulator is not probably the right tool to investigate GaAs device behavior beyond SOA – as it does not take into account the destruction of the crystal structure. The results of diffusion are most possibly correct.

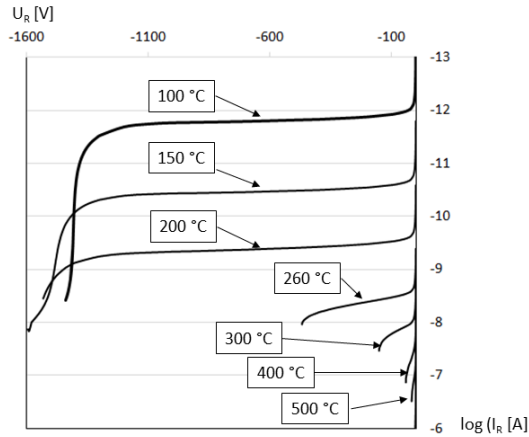


Figure 9: Reverse IV characteristics at different temperatures.

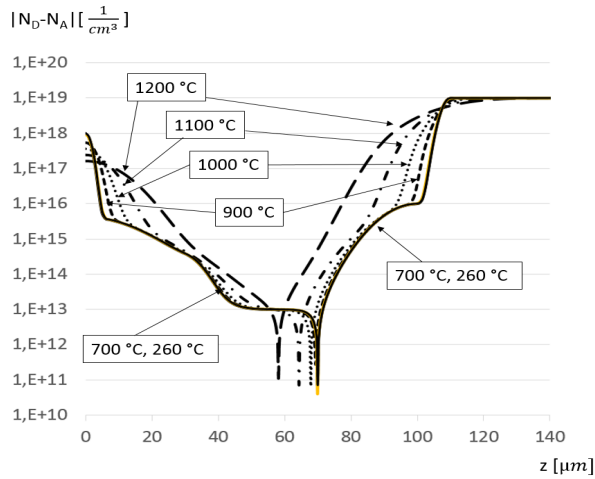


Figure 10: The simulated influence of annealing for 416 days at different temperatures on the doping profile of the simulated device.

5 Conclusions

Based on the currently available simulation models the potential failure of operation of the device could occur when the body of the diode package is not sufficiently cooled, reaching operating area where failure occurs due to device physics (increase of currents, inability to withstand reverse voltage) than thermal burnout. The abnormal high temperature must last for a long time to change the device internal structure through diffusion of impurities. The semiconductor process simulator used for the investigation of the annealing influence does not take destruction of the crystal lattice into account – so this should be investigated further with possible other tools.

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