Numerical analysis of the influence of deep energy level traps in SiC Schottky structures

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Abstract

The Thomas Johann Seebeck Department of Electronics at the Tallinn University of Technology has studied the properties of Schottky contacts since the 1980s. The theoretical studies have been accompanied by analytical and numerical computer simulations. Realisation of SiC complementary power Schottky diodes has been possible since 1994, using diffusion welding (DW) metallisation technology. Measurement of the electrical properties of the produced samples offers excellent possibility to verify and enhance computer models, and as feedback provides possible explanations to phenomenon found in the measurement results.

This paper provides a comparison between measured and simulated results for SiC Schottky power diode structures. The paper addresses the simulation results investigating the influence of deep energy traps and/or defects on electrical characteristics of SiC Schottky diodes manufactured using DW metallisation technology. The numerical model includes the exact model for describing the behaviour of deep energy traps in the epitaxial layer. The analysis takes into account the influence of ambient temperature on static characteristics of the device. The outcome of this particular research is addressed for the optimisation of the switching devices applied in the power converters, with the aim of reducing the general energy consumption in different power grids.
Keywords: silicon carbide, metal semiconductor contacts, diffusion welding, interface layer, deep energy levels, DLTS method, numerical modelling, Schottky diodes.

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1 Introduction

Silicon carbide (SiC) is an outstanding wide bandgap semiconductor material with good physical properties. Although the first uses of the material in electronics (radio detectors, LEDs) date back to the beginning of the 20th century, the once proposed wide usage in power semiconductor electronics has not come true. This has been due to difficulties in the production of homogenous devices with large working surfaces, resulting in low yield and the relatively high cost of the production process. SiC has gained much more popularity in the industry as a material for excellent blue LEDs. The physical and electrical properties of SiC have been carefully studied since the 1960s. Most technologies currently used to produce SiC devices were empirically developed rather than based on a solid theoretical background. The developments of high-speed power devices based on SiC over the last few decades has paid special attention to junction-barrier Schottky (JBS) diodes, in which regions of *pn*- and Schottky barrier (SB) junctions are alternated in short periods of a few to several μm [1–3]. The advantages of the JBS diodes are SB-diode-like forward characteristics with low turn-on voltages and *pn*-diode-like reverse characteristics with low current leakage. Furthermore, the JBS diodes operate at a lower voltage than the turn-on voltage of the *pn*-junction, and exhibit faster switching speeds in comparison with that of pin diodes due to the absence of minority carrier injection.

The metal–semiconductor interface is one of the fundamental blocks in any semiconductor device technology. Metal contacts, when Ohmic, are used for electrical terminals to devices. When the dopant concentration is sufficiently low and the work-functions of metal and SiC are sufficiently different, metal contacts possess rectifying characteristics, and so called Schottky contacts have been created. The Thomas Johann Seebeck Department of Electronics at the Tallinn University of Technology has studied the properties of Schottky contacts since the 1980s. The theoretical studies were accompanied by analytical and numerical computer simulations. Furthermore, the local production of SiC power Schottky diodes has been possible, using diffusion welding (DW) metallisation technology. The measurement of electrical properties of the produced samples offers excellent possibilities to verify and enhance computer models, and as feedback provides possible explanations to anomalies found in the process of measurements. In our earlier papers [4, 5] we have stated that structures fabricated on *p*-type SiC have some unique characteristics, which are particularly promising for high current density and high temperature applications.

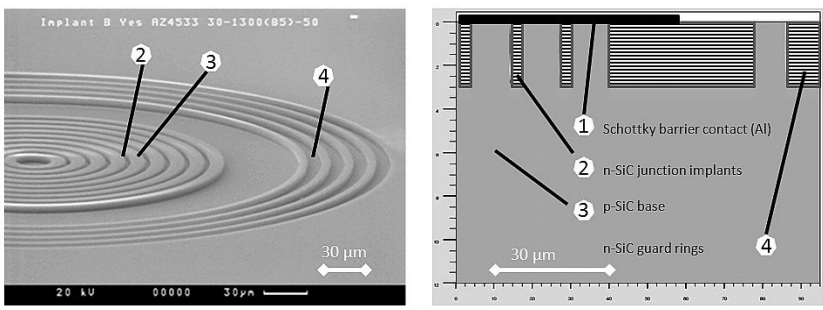
Over the last few years, several reports and experimental studies have been carried out on the deep energy level in n-and p-layers of 6H- and 4H-SiC Schottky and *pn*-diodes [6–9]. For example the results of experimental studies on deep levels in the *p*-base of 6*H*-SiC diodes show an unknown origin of deep levels, with ionisation energy of E_c-1.45eV, which acts as an effective recombination centre for minority carriers, and controls recombination processes. In our last work [10] we showed for the first time that the non-regular behaviour of static characteristics of Schottky diodes could be related to the influence of

deep energy levels in epilayers created during the diffusion welding metallisation process of semiconductor devices. It is agreed that midcap levels act as efficient carrier generation and recombination centres, being possible lifetime killers. On the other hand, in high-quality *n*-type 4H-SiC epilayers the capture cross-section of two defects (deep centres like E_c-0.65eV) [11] and E_c-1.55eV) are shown to be temperature independent, which indicates a lesser influence on electrical characteristics from this side, but they seem to assist multi-phonon emission.

In this paper we provide a comparison between measured and simulated results for SiC Schottky power diode structures. The paper addresses the simulation results investigating the influence of device geometry fluctuations, deep energy traps and/or defects on electrical characteristics of SiC Schottky diodes with improved geometry and specific guard rings manufactured using DW metallisation technology. The numerical model includes the exact model for describing the behaviour of deep energy traps in the epitaxial layer. The analysis takes into account the influence of ambient temperature on the static and dynamic characteristics of the device. The outcome of this particular research is addressed for the optimisation of switching devices applied in power converters with the aim of reducing the general energy consumption in different power grids.

2 Description of the problem

The geometry of DW Al Schottky-contact diodes with protective *pn*-junction rings is shown on Figure 1 and described with material parameters in [1].



(1) (2)

Figure 1: (1) Electron microscope image of the real JBS diode structure (from [1]), (2) 2-D substructure used in simulations.

The results of the measurements of the Junction Barrier Schottky (JBS) diodes forward *I-V* characteristics of complementary diodes are shown in Figure 2 (based on the data that was the basis of publication [4]).

As seen from Figure 2 (1), the forward *I-V* characteristics temperature dependence on *n*-substrate JBS is as expected, the rise in temperature shifts the characteristics towards a higher voltage drop on the structure. The JBS diodes on

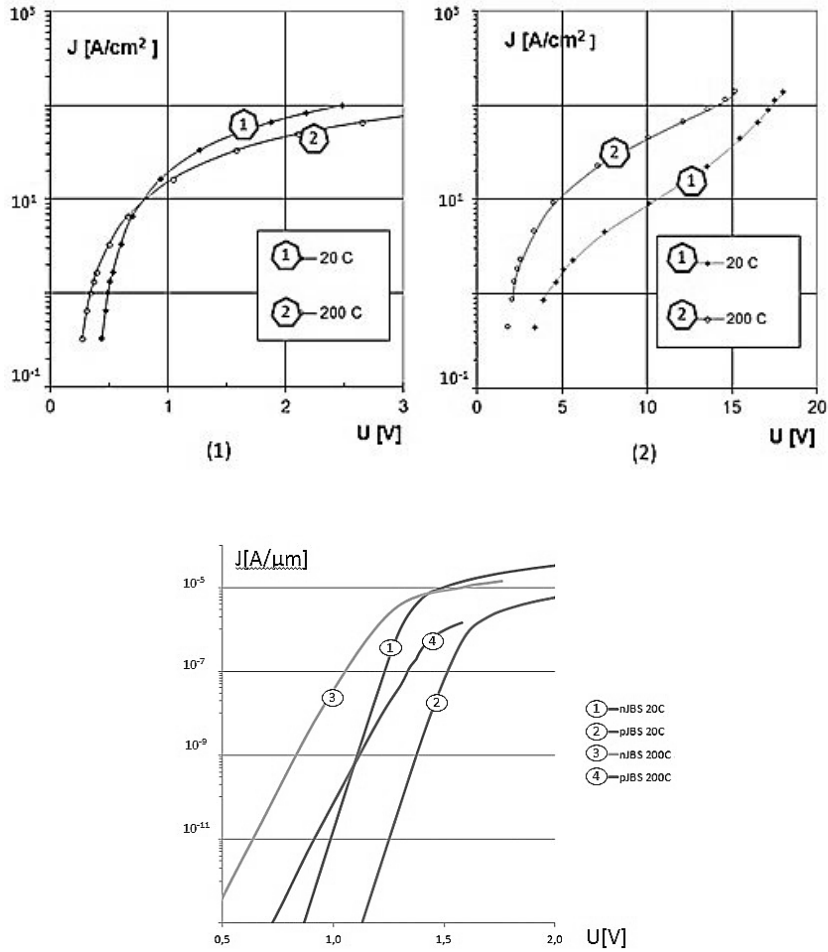


Figure 2: Measurement results (upper figures); (1) *n*-substrate SiC JBS diode (higher temperature causes higher voltage drop on diode). (2) *p*-substrate SiC JBS diode (higher temperature causes lower voltage drop on diode). simulation results (lower figure).

the *p*-SiC substrate (Figure 2 (2)) acts unexpectedly to the contrary, a higher device temperature causes a lowering of the voltage drop on the device.

Using the Silvaco device simulator ATLAS, an attempt was made to verify the results [2]. Simulations verified the behaviour of JBS diodes based on *n*-SiC but did not confirm the measurement results for *p*-SiC devices. In simulations, both complementary structures revealed the same kind of temperature dependence, as seen in the lower part of Figure 2.

Various reasons for the difference in temperature dependence between *n*-substrate and *p*-substrate JBS were considered and tested in simulations. A

change in simulated substructure geometry (relations between Schottky and barrier widths) revealed that the geometry was not the cause of the effect investigated. As an interesting side-effect, an uneven current distribution was observed for both *n*-substrate and *p*-substrate devices, even at modest current densities (Figure 3). This could result in local overheating and possibly subsequent contact degradation.

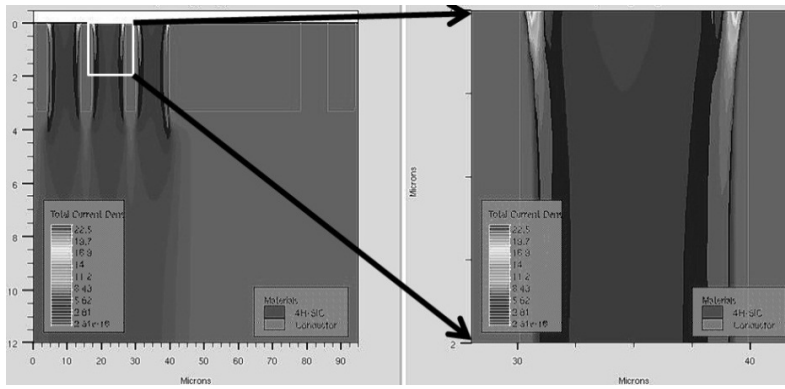


Figure 3: Uneven current distribution in *p*-substrate JBS at forward current density 1A/cm^2.

In Transmission Electron Microscope (TEM) studies of subcontact layers in SiC after the DW process it appears that between the Al contact and SiC an approximately 5–25 nm interface layer has formed, as shown in Figure 3 [5]. Shear micro deformations have taken place, and as a result plane inclusions of small-grained phase have appeared. Further decipherment of electron diffraction patterns shows the presence of SiC, Si C (graphite) and Al inclusion planes.

The abovementioned interface layer between the Al Schottky contact and SiC could possibly be the cause of the odd behaviour of the *p*-SiC forward *I-V* characteristics. The influence of the layer could be simulated by including the deep trap's influence on the recombination process.

Of the different deep trap levels the following influences were studied: *n*-impurity centre (as *p*-SiC is *n*-doped), donor traps at 0.085eV and 0.125eV levels; Al impurity centre, acceptor traps at 0.27eV level; B impurity centre, acceptor traps at 0.39eV level; D centre, acceptor traps at E_v+0.85eV level; *i*-centre, traps at E_v+0.52eV level; Z_1 centre, traps at E_c-0.62eV level; Z_2 centre, traps at E_c-0.64eV level [12]. Additionally, the following levels controlling the recombination process are mentioned: E_c-0.35eV, E_c-1.45ev [6]. The other impurities and production technology-generated trap levels should not be relevant to the materials and processes used in the current case. Even boron impurity should be irrelevant in *p*-SiC, but was included as it was used in the production of the complementary *n*-SiC Schottky diode.

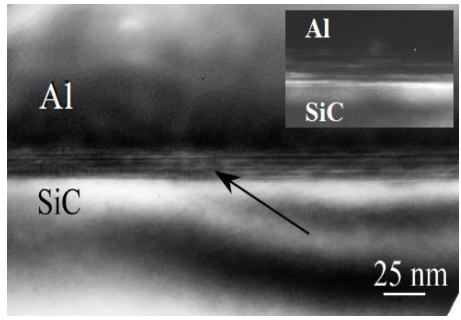


Figure 4: TEM image showing the interface layer that has formed between the Al contact and SiC during the process of diffusion welding.

For the simulation set-up a very simple structure was used in order to investigate the influence of the trap type and position in the energy bandgap, concentration and effective capture cross-section to the *p*-SiC Schottky diode *I-V* characteristics. The structure has a thin surface layer under the Al Schottky electrode, where the influence of deep traps is modified during the series of simulations, a low-doped buffer layer (N_d=2×10^{15}cm^{-3}) of 5 micrometres and an additional hi-doped buffer layer for achieving Ohmic contact with Al at the other end of the simulated device. A Silvaco ATLAS simulator, that solves the set of basic semiconductor equations, is used for the calculations.

To model the deep level traps and defects, the modified Poisson's equation is used:

$$div(\varepsilon \nabla \psi) = q\left(n - p - N_D^+ + N_A^-\right) - Q_T \tag{1}$$

where ε is the permittivity, ψ is the potential, q is the electron charge, n and p are charge carriers, and N_D^+ and N_A^- are ionised impurity concentrations, and Q_T describes the charge due to traps and defects.

The presence of traps and defects may significantly influence the electrical characteristics of the device. The traps with their associated energy (additional energy levels in forbidden gap) exchange the charge with the conduction or valence band through the emission processes, which changes the recombination rate (statistics) inside the bulk semiconductor material. The donor and acceptor type traps' density determines:

$$Q_T = q\left(N_{tD}^+ - N_{tA}^-\right) \tag{2}$$

where N_{tD}^+ and N_{tA}^- are the densities of the ionised donor-like and acceptor-like traps respectively, and the total charge (the density of traps) determines:

$$N_{tD}^+ = \sum_{\alpha=1}^{k} N_{tD\alpha}^+ \,,\; N_{tA}^- = \sum_{\beta=1}^{m} N_{tA\beta}^- \tag{3}$$

where k and m are the number of donor- and acceptor-like traps, respectively.

The probability of ionisation is calculated under the assumption that the capture cross-sections are constant for all energy levels, which is concluded from the results of the analysis given in [13]. The further described algorithm is realised through the modified Shockley-Read-Hall (SRH) recombination model. The trap assisted tunnelling is described via the model based on the analysis presented in [14], which additionally modifies the SRH recombination model introducing the enhancement factors. The enhancement factor also includes the probability of tunnelling process. Finally, barrier lowering must be taken into account. Barrier lowering is obtained from the Coulomb interaction of electrons. The model describing the process is based on results published in [15, 16]. The Silvaco ATLAS simulator used includes the mathematical models describing almost all shortly discussed phenomena, and on this basis the numerical algorithm for investigating the influence of deep level traps on the electrical characteristics of *p*-SiC Schottky structures has been developed and applied.

3 Results and discussion

The first series of simulations (trap levels acting as acceptors: Al, B, Z-centres, recombination centres and trap levels acting as donors: *N*, *i*-centre, recombination centres) revealed that acceptor traps have practically no influence at all on the forward *I-V* characteristics within reasonable parameter values of density, carrier capture cross-section and degeneracy factors of the trap centre. The influence of donor-like traps is observable. Simulations the where trap carrier capture cross-sections were changed between $1\times10^{15}\text{cm}^{-2}$ and $1\times10^{17}\text{cm}^{-2}$ revealed that this parameter does not have a noticeable influence on forward *I-V* characteristics.

The influence of trap concentration at room temperature depends greatly on the trap location. At E_v+0.125 the trap concentrations influence becomes noticeable from a trap density of $1\times10^{17}\text{cm}^{-3}$ (Figure 5, left), and the forward *I-V* characteristics of 20°C practically coincide with the *I-V* characteristics of 200°C at a density of $1\times10^{18}\text{cm}^{-3}$ (not shown in the Figure). The influence window for the E_v+0.52 trap lies between density levels of $1\times10^{15}\text{cm}^{-2}$ (where the influence is unnoticeable) and $1\times10^{16}\text{cm}^{-3}$ (where traps have totally shut down the current) (Figure 5, right).

The influence of the trap level location at lower temperatures is significant. In current simulations the trap level close to the valence band edge (*N*, E_v+0.085eV) practically did not have an influence on *I-V* characteristics despite the high density ($1\times10^{18}\text{cm}^{-3}$). Trap levels farther from the edge (*N*, E_v+0.125eV) practically brought *I-V* characteristics simulated at temperatures of 20°C, 200°C and 400°C together. At temperatures higher than 200°C, the simulated forward *I-V* characteristics for trap levels E_v+0.085eV and E_v+0.125eV practically coincided. Deeper traps, regardless of the simulation temperature (E_v+0.52eV) at the abovementioned high density, completely shut the current down (Figure 6).

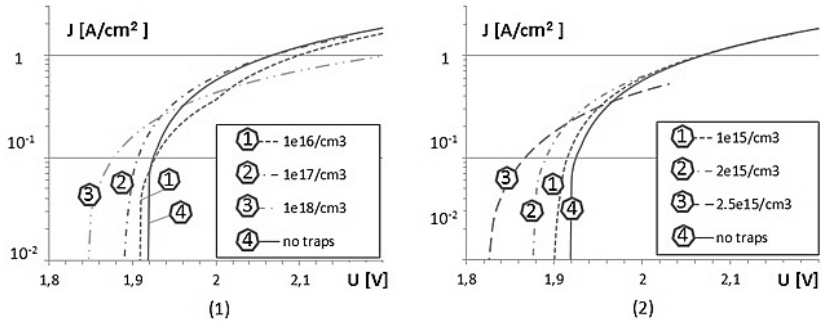


Figure 5: Trap density influence on *I-V* characteristics at 20°C. (1) simulation results with trap level E_v+0.125eV. (2) simulation results with trap level E_v+0.52eV. traps closer to the centre of the bandgap needed lower concentrations to influence the *I-V* characteristics.

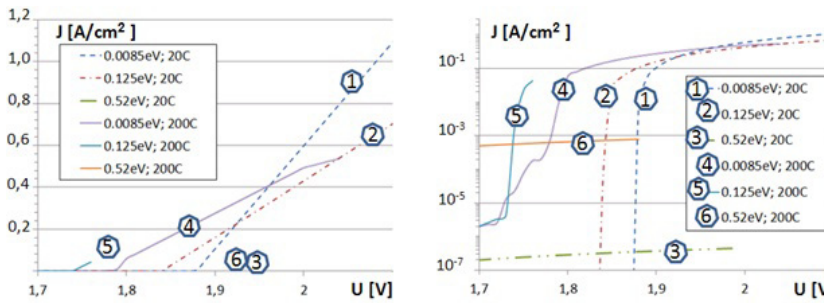


Figure 6: Different level deep trap influence on *I-V* characteristics at temperatures of 20ºC and 200ºC (in logarithmic scale on the right). The trap concentration used in the simulations is 1×10^{18}cm^{-3}.

The behaviour of Schottky diodes on *p*-SiC substrate could be reproduced by simulations, when the influence of the deep traps was taken into account in the recombination processes. Of the different deep trap levels [5], only those that are relevant to *p*-SiC or production technology were investigated.

4 Conclusions

The simulations indicated that the mechanism behind the forward *I-V* characteristics temperature dependency anomaly for *p*-SiC Schottky diodes could be deep donor-like traps. These traps are most probably caused by material deformations during the diffusion welding process. The interface layer seen in TEM supports this hypothesis.

To have an influence of the amount seen in the measured forward *I-V* characteristics the traps should be located higher from valence zone edge than 0.125eV (the higher the level, the greater the influence) and the density of the

traps should be significant, in the range of $1\times10^{17}\text{cm}^{-3}$ or more. Further investigations are needed; both DLTS measurements to determine the trap locations and further simulations to adjust trap levels and densities to match the measurement results.

The reason why the influence of deep traps decreases with the rise in temperature is not sufficiently clear. One reason could be that with the rise in temperature the effective carrier capture cross-section decreases. Another reason could be that at lower temperatures, positively charged donor traps create an additional space charge that influences the hole-current through the creation of an additional electric field and/or influencing Schottky barrier properties (e.g. height).

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